


PROTO :

SYNC MASTER=K901 MLB

SYNC DATE=02/15/2011

Revision History

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051-9058

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SIZE
D

Functional Test Points

D

Fan Connectors

612	TRUE	PP5V_S0	6 7
615	TRUE	FAN_RT_PWM	52
616	TRUE	FAN_RT_TACH	52
(NEED TO ADD 1 GND TP)			

MIC_FUNC_TEST

650	TRUE	BI_MIC_LO	61 62
650	TRUE	BI_MIC_HI	61 62
650	TRUE	BI_MIC_SHIELD	61 62
(NEED TO ADD 1 GND TP)			

SPEAKER_FUNC_TEST

660	TRUE	SPKRAMP_L_N_OUT	60 61 85
660	TRUE	SPKRAMP_L_P_OUT	60 61 85
660	TRUE	SPKRAMP_R_N_OUT	60 61 85
660	TRUE	SPKRAMP_R_P_OUT	60 61 85
660	TRUE	SPKRAMP_SUB_N_OUT	60 61 85
660	TRUE	SPKRAMP_SUB_P_OUT	60 61 85

LVDS_FUNC_TEST

620	TRUE	PP3V3_LCDVDD_SW_F (NEED 2 TP)	6 74
620	TRUE	PP3V3_S0_LCD_F	6 74
620	TRUE	PPVOUT_SW_LCDBKLT (NEED 2 TP)	74 77
620	TRUE	LVDS_DDC_CLK	8 74
620	TRUE	LVDS_DDC_DATA	8 74
620	TRUE	LVDS_IG_A_DATA_N<0>	17 74 80
620	TRUE	LVDS_IG_A_DATA_P<0>	17 74 80
620	TRUE	LVDS_IG_A_DATA_N<1>	17 74 80
620	TRUE	LVDS_IG_A_DATA_P<1>	17 74 80
620	TRUE	LVDS_IG_A_DATA_N<2>	17 74 80
620	TRUE	LVDS_IG_A_DATA_P<2>	17 74 80
620	TRUE	LVDS_CONN_A_CLK_F_N	74 85
620	TRUE	LVDS_CONN_A_CLK_F_P	74 85
620	TRUE	LED_RETURN_1	74 77
620	TRUE	LED_RETURN_2	74 77
620	TRUE	LED_RETURN_3	74 77
620	TRUE	LED_RETURN_4	74 77
620	TRUE	LED_RETURN_5	74 77
620	TRUE	LED_RETURN_6	74 77
(NEED TO ADD 5 GND TP)			

SATA_ODD_CONN

664	TRUE	PP5V_SW_ODD (NEED 2 TP)	6 41
660	TRUE	SMC_ODD_DETECT	41 45
660	TRUE	SATA_ODD_D2R_C_P	41 85
660	TRUE	SATA_ODD_D2R_C_N	41 85
660	TRUE	SATA_ODD_R2D_P	41 80
660	TRUE	SATA_ODD_R2D_N	41 80
660	TRUE	SMC_SSD_TEMP_CTL_R	
660	TRUE	HDD_OOB_TEMP	
(NEED TO ADD 3 GND TP)			

SATA_HDD/IR/SIL

660	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	6 41
660	TRUE	SATA_HDD_R2D_P	41 80
660	TRUE	SATA_HDD_R2D_N	41 80
660	TRUE	SATA_HDD_D2R_C_P	41 80
660	TRUE	SATA_HDD_D2R_C_N	41 80
660	TRUE	SYS_LED_ANODE_R	
660	TRUE	IR_RX_OUT	41 44
660	TRUE	SMC_SSD_THROTTLE_R	
660	TRUE	PP5V_S3_IR_R	41
(NEED TO ADD 3 GND TP)			

BATT_POWER_CONN

660	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
660	TRUE	SYS_DETECT_L	63
660	TRUE	PPVBAT_G3H_CONN (NEED 5 TP)	63 64
(NEED TO ADD 5 GND TP)			

BIL_CONN

660	TRUE	PP3V42_G3H	6 7
660	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
660	TRUE	SMC_BIL_BUTTON_L	45 46 63
660	TRUE	SMC_LID_R	63
(NEED TO ADD 2 GND TP)			

X19_CONN

660	TRUE	PP3V3_WLAN (NEED 3 TP)	6 32 46
660	TRUE	PCIE_AP_D2R_PI_P	32 81
660	TRUE	PCIE_AP_D2R_PI_N	32 81
660	TRUE	PCIE_AP_R2D_P	32 81
660	TRUE	PCIE_AP_R2D_N	32 81
660	TRUE	PCIE_CLK100M_AP_CONN_P	32 85
660	TRUE	PCIE_CLK100M_AP_CONN_N	32 85
660	TRUE	PP3V3_S3RS4_BT_F	32
660	TRUE	PCIE_WAKE_L	17 24 32
660	TRUE	USB_BT_CONN_P	32 80
660	TRUE	USB_BT_CONN_N	32 80
660	TRUE	AP_CLKREQ_Q_L	32
660	TRUE	AP_RESET_CONN_L	32
660	TRUE	AP_TEMP_SMB_SDA_R	32
660	TRUE	AP_TEMP_SMB_SCL_R	32
660	TRUE	WIFI_EVENT_L_R	32
(NEED TO ADD 5 GND TP)			

IPD_FLEX_CONN

660	TRUE	PP3V3_S4	6 7
660	TRUE	PP18V5_Z2	6 54
660	TRUE	Z2_CS_L	53 54
660	TRUE	Z2_DEBUG3	53 54
660	TRUE	Z2_MOS1	53 54
660	TRUE	Z2_MISO	53 54
660	TRUE	Z2_SCLK	53 54
660	TRUE	Z2_BOOST_EN	54
660	TRUE	Z2_HOST_INTN	53 54
660	TRUE	Z2_CLKIN	53 54
660	TRUE	Z2_KEY_ACT_L	53 54
660	TRUE	Z2_RESET	53 54
660	TRUE	PSOC_MISO	53 54
660	TRUE	PSOC_MOSI	53 54
660	TRUE	PSOC_SCLK	53 54
660	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
660	TRUE	PSOC_F_CS_L	53 54
660	TRUE	PICKB_L	53 54
660	TRUE	PP5V_S5_CUMULUS	54
(NEED TO ADD 2 GND TP)			

KEYBOARD_CONN

660	TRUE	PP3V3_S4	6 7
660	TRUE	PP3V42_G3H	6 7
660	TRUE	WS_KBD1	53
660	TRUE	WS_KBD2	53
660	TRUE	WS_KBD3	53
660	TRUE	WS_KBD5	53
660	TRUE	WS_KBD6	53
660	TRUE	WS_KBD7	53
660	TRUE	WS_KBD8	53
660	TRUE	WS_KBD9	53
660	TRUE	WS_KBD10	53
660	TRUE	WS_KBD11	53
660	TRUE	WS_KBD12	53
660	TRUE	WS_KBD13	53
660	TRUE	WS_KBD14	53
660	TRUE	WS_KBD15_CAP	53
660	TRUE	WS_KBD16_NUM	53
660	TRUE	WS_KBD17	53
660	TRUE	WS_KBD18	53
660	TRUE	WS_KBD19	53
660	TRUE	WS_KBD20	53
660	TRUE	WS_KBD21	53
660	TRUE	WS_KBD22	53
660	TRUE	WS_KBD23	53
660	TRUE	WS_KBD_ONOFF_L	53
660	TRUE	WS_LEFT_SHIFT_KBD	53
660	TRUE	WS_LEFT_OPTION_KBD	53
660	TRUE	WS_CONTROL_KBD	53
(NEED TO ADD 2 GND TP)			

KBD_BACKLIGHT_CONN

660	TRUE	KBDLED_ANODE	54
660	TRUE	SMC_KBDLED_PRESENT_L	54
(NEED TO ADD 1 GND TP)			

CAMERA/ALS_CONN

660	TRUE	PP5V_S3_ALSCAMERA_F	32
660	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
660	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
660	TRUE	USB_CAMERA_CONN_P	32 80
660	TRUE	USB_CAMERA_CONN_N	32 80
(NEED TO ADD 2 GND TP)			

DEBUG_VOLTAGE

660	TRUE	PPVCORE_S0_CPU	7
660	TRUE	PPVCORE_S0_AXG	7
660	TRUE	PP1V2_S3_ENET_INTREG	71
660	TRUE	PP1V05_S0	7
660	TRUE	PP1V5_S3RS0	7 85
660	TRUE	PP1V8_S0	7
660	TRUE	PP3V3_S0	7 85
660	TRUE	PP5V_S0	6 7
660	TRUE	PP3V3_S3	7
660	TRUE	PP5V_S3	7
660	TRUE	PPVCCSA_S0_CPU	7
660	TRUE	PP3V3_S5	7 85
660	TRUE	PP3V42_G3H	6 7
660	TRUE	PPBUS_G3H	7
660	TRUE	PP3V3_ENET	7
660	TRUE	PP3V3_WLAN	6 32 46
660	TRUE	PP5V_SW_ODD	6 41
660	TRUE	PP5V_S0_HDD_FLT	6 41
660	TRUE	PP18V5_Z2	6 54
660	TRUE	PP3V3_S0_LCD_F	6 74
660	TRUE	PP3V3_LCDVDD_SW_F	6 74
660	TRUE	PP4V5_AUDIO_ANALOG	57 62
660	TRUE	PP1V5_S3	7
660	TRUE	SMC_PM_G2_EN	45 73
660	TRUE	PM_SLP_S4_L	17 26 32 45 73
660	TRUE	PM_SLP_S3_L	8 17 26 45 73
(NEED TO ADD 6 GND TP)			

DC_POWER_CONN

660	TRUE	PP18V5_DCIN_FUSE (NEED 3 TP)	63
660	TRUE	ADAPTER_SENSE	63
(NEED TO ADD 4 GND TP)			

LPC+SPI_DEBUG_CONN

660	TRUE	LEC_AD<0>	16 45 47 81
660	TRUE	LPC_AD<1>	16 45 47 81
660	TRUE	LPC_AD<2>	16 45 47 81
660	TRUE	LPC_AD<3>	16 45 47 81
660	TRUE	LPC_CLK33M_LPCPLUS	24 47 81
660	TRUE	LPC_FRAME_L	16 45 47 81
660	TRUE	LPC_PWRDWN_L	17 45 47
660	TRUE	LPC_SERIRO	16 45 47
660	TRUE	LPCPLUS_GPIO	19 47
660	TRUE	LPCPLUS_RESET_L	24 47
660	TRUE	PM_CLKRUN_L	17 45 47
660	TRUE	PP3V42_G3H	6 7
660	TRUE	PP5V_S0	6 7
660	TRUE	SMC_RX_L	45 46 47
660	TRUE	SMC_TCK	45 46 47
660	TRUE	SMC_TDI	45 46 47
660	TRUE	SMC_TDO	45 46 47
660	TRUE	SMC_TMS	45 46 47
660	TRUE	SMC_TX_L	45 46 47
660	TRUE	SPI_ALT_CLK	47
660	TRUE	SPI_ALT_CS_L	47
660	TRUE	SPI_ALT_MISO	47
660	TRUE	SPI_ALT_MOSI	47
660	TRUE	SPIROM_USE_MLB	19 47 56
(NEED TO ADD 2 GND TP)			

NC_NO_TESTS

17	TP_CRT_IG_BLUE	==	TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	==	MAKE_BASE=TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	==	MAKE_BASE=TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	==	TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	==	MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	==	TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	==	MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
17	TP_LVDS_IG_CTRL_CLK	==	TRUE	NC_LVDS_IG_CTRL_CLK
17	TP_LVDS_IG_CTRL_DATA	==	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
17	TP_PCH_LVDS_VBG	==	MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	==	TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	==	MAKE_BASE=TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	==	MAKE_BASE=TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	==	TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	==	MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3

16	TP_CLINK_CLK	==	TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	==	MAKE_BASE=TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	==	MAKE_BASE=TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	==	TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	==	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP

38	TP_FW643_SDA	==	TRUE	NC_FW643_SDA
38	TP_FW643_SM	==	MAKE_BASE=TRUE	NC_FW643_SM
38	TP_FW643_TCK	==	TRUE	NC_FW643_TCK
38	TP_FW643_TMS	==	MAKE_BASE=TRUE	NC_FW643_TMS
38	TP_FW643_FW620_L	==	TRUE	NC_FW643_FW620_L
38	TP_FW643_VBUE	==	MAKE_BASE=TRUE	NC_FW643_VBUE
38	TP_FW643_OCR10_CTL	==	TRUE	NC_FW643_OCR10_CTL
38	TP_FW643_AVREG	==	TRUE	NC_FW643_AVREG
38	TP_FW643_TDI	==	MAKE_BASE=TRUE	NC_FW643_TDI

23	TP_XDP_PCH_OBSFN_A<0..1>	==	TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	==	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDP_PCH_HOOK2	==	TRUE	NC_TP_XDP_PCH_HOOK2
23	TP_XDP_PCH_HOOK3	==	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	==	TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	==	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	==	TRUE	NC_TP_XDP_PCH_HOOK5

16	TP_PCH_GPIO64_CLKOUTFLEX0	==	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	==	MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	==	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	==	MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

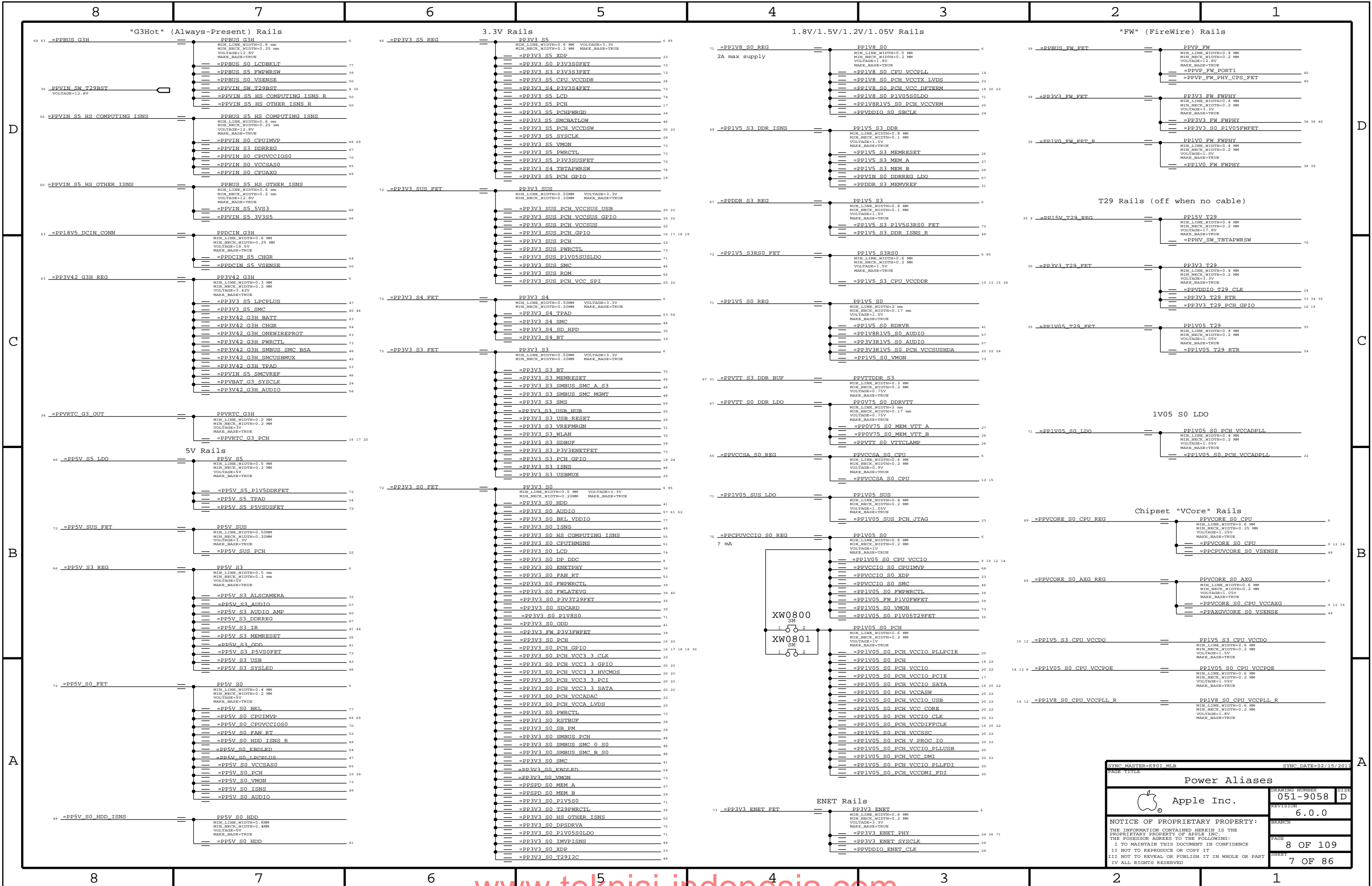
NC_NO_TESTS

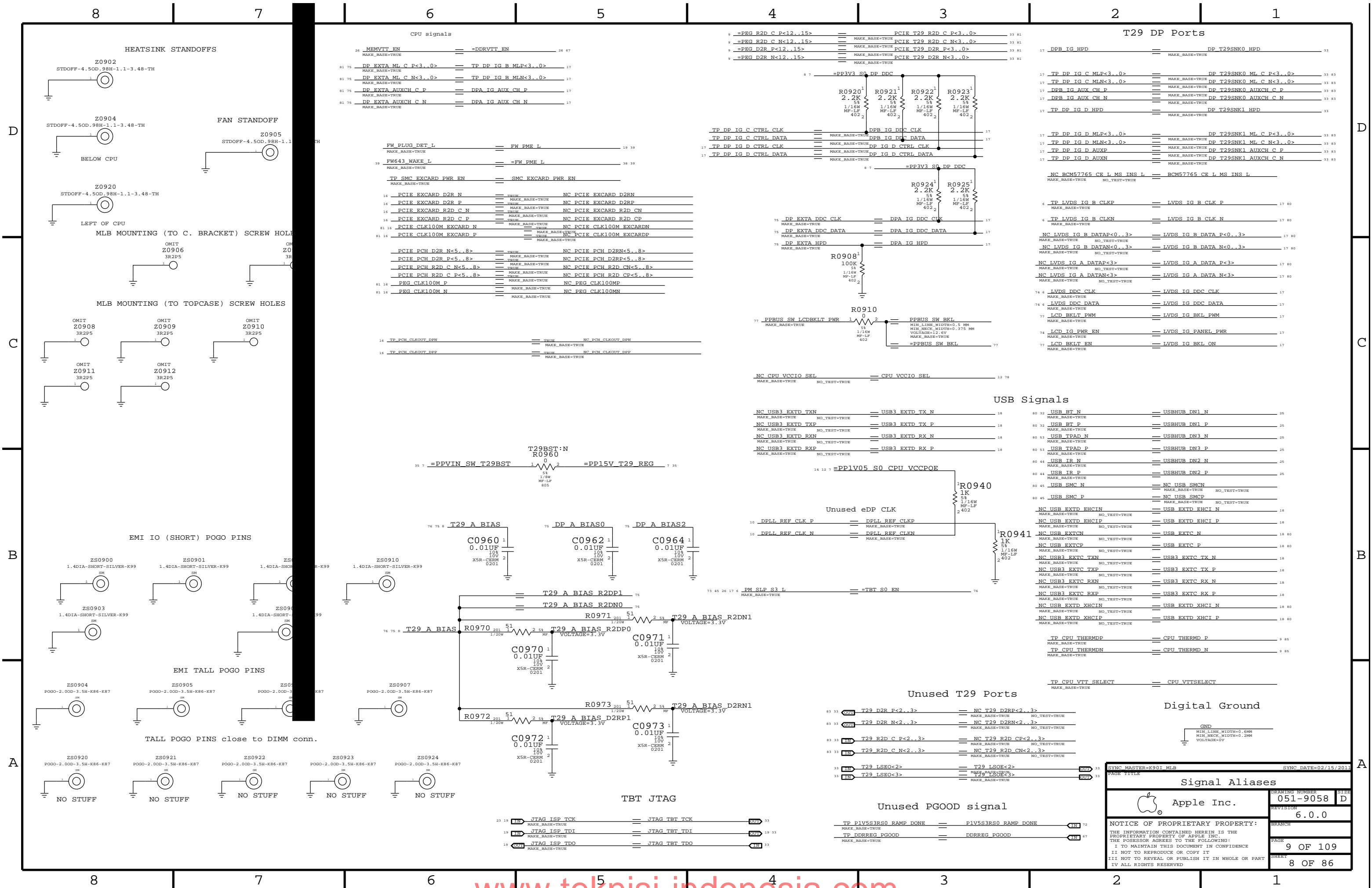
660	TRUE	NC_FW2_TBPB	40
660	TRUE	NC_FW2_TPNB	40
660	TRUE	NC_FW2_TPBAS	40
660	TRUE	NC_FW2_TPAP	40
660	TRUE	NC_FW2_TPAN	40
660	TRUE	NC_FW0_TBPB	40
660	TRUE	NC_FW0_TPNB	40
660	TRUE	NC_FW0_TPAP	40

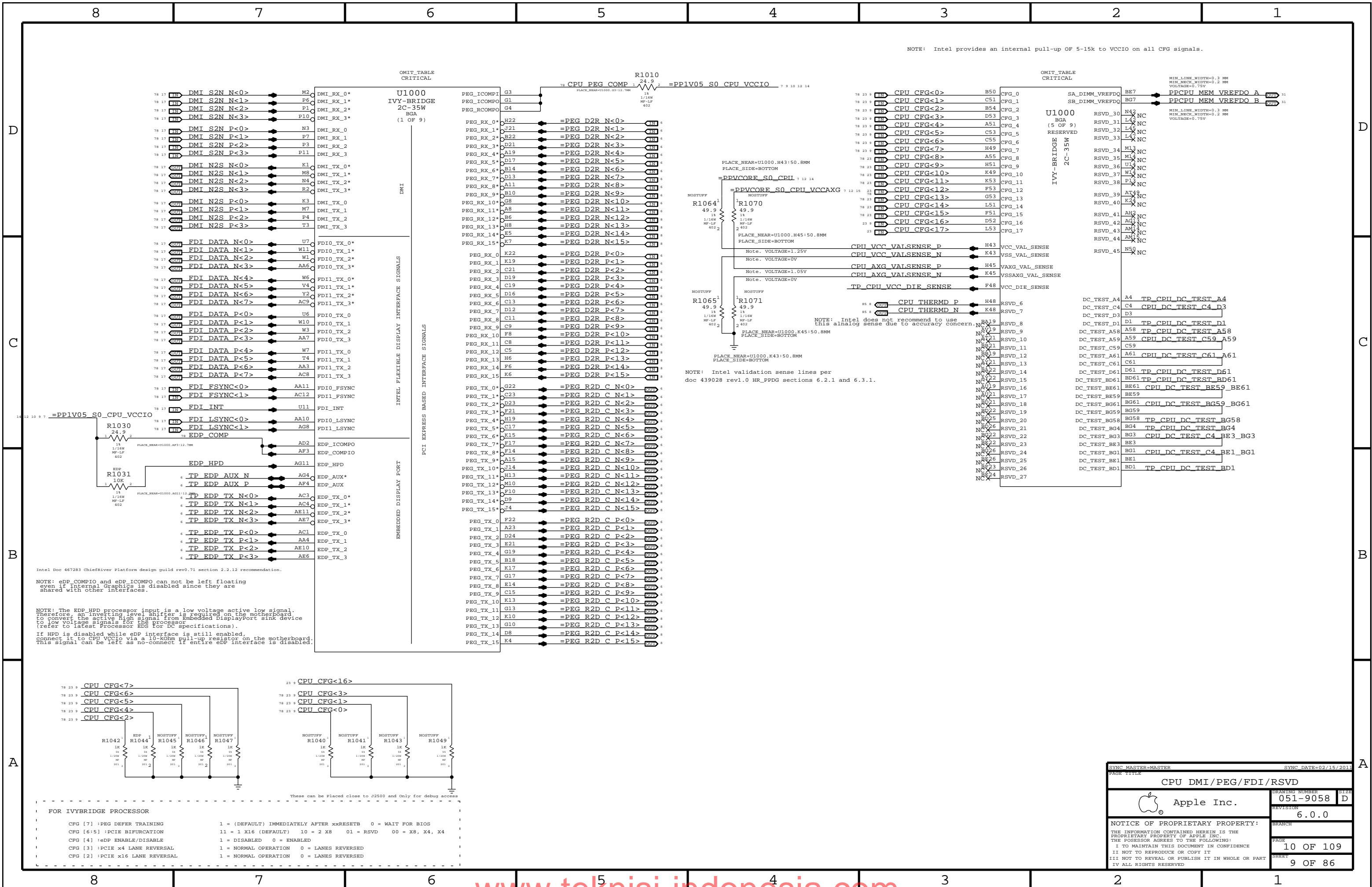
660	TRUE	XDP_PCH_AP_PWR_EN	
660	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	
660	TRUE	XDP_PCH_SDCONN_STATE_RST_L	
660	TRUE	XDP_PCH_ENET_PWR_EN	
660	TRUE	XDP_PCH_SDCONN_DET_L	
660	TRUE	XDP_PCH_S5_PWRGD	23
660	TRUE	XDP_PCH_PWRBTN_L	23
660	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	
660	TRUE	XDP_FW_CLKREQ_L	
660	TRUE	XDP_AP_CLKREQ_L	
660	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	

17	TP_SDVO_TVCLKINN	==	TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	==	MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	==	TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	==	MAKE_BASE=TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	==	TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	==	MAKE_BASE=TRUE	NC_SDVO_INTP

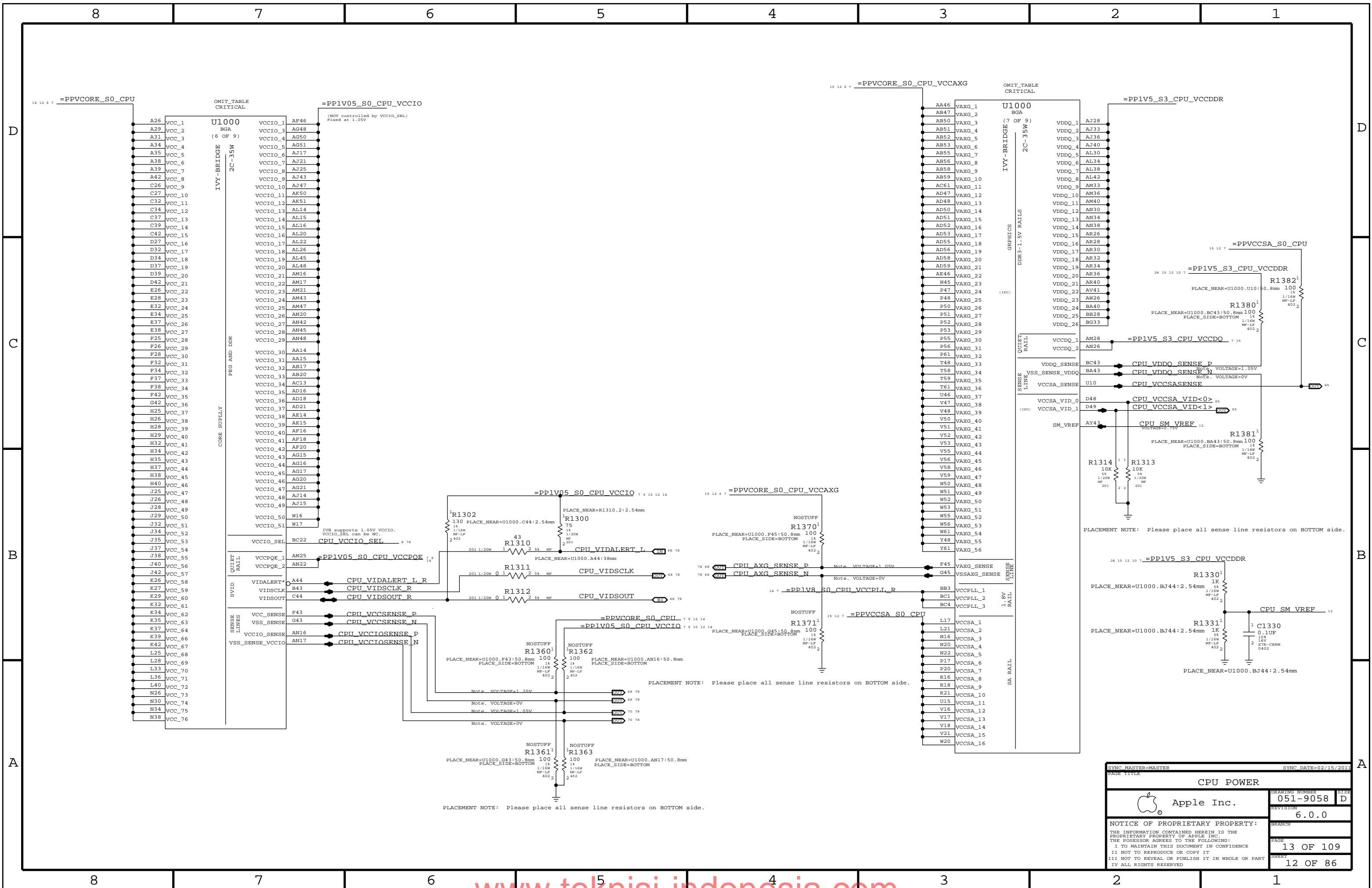
NC_EDP_TXP<0..3>	==	TRUE	TP_EDP_TX_P<0..3>
NC_EDP_TXN<0..3>	==	TRUE	TP




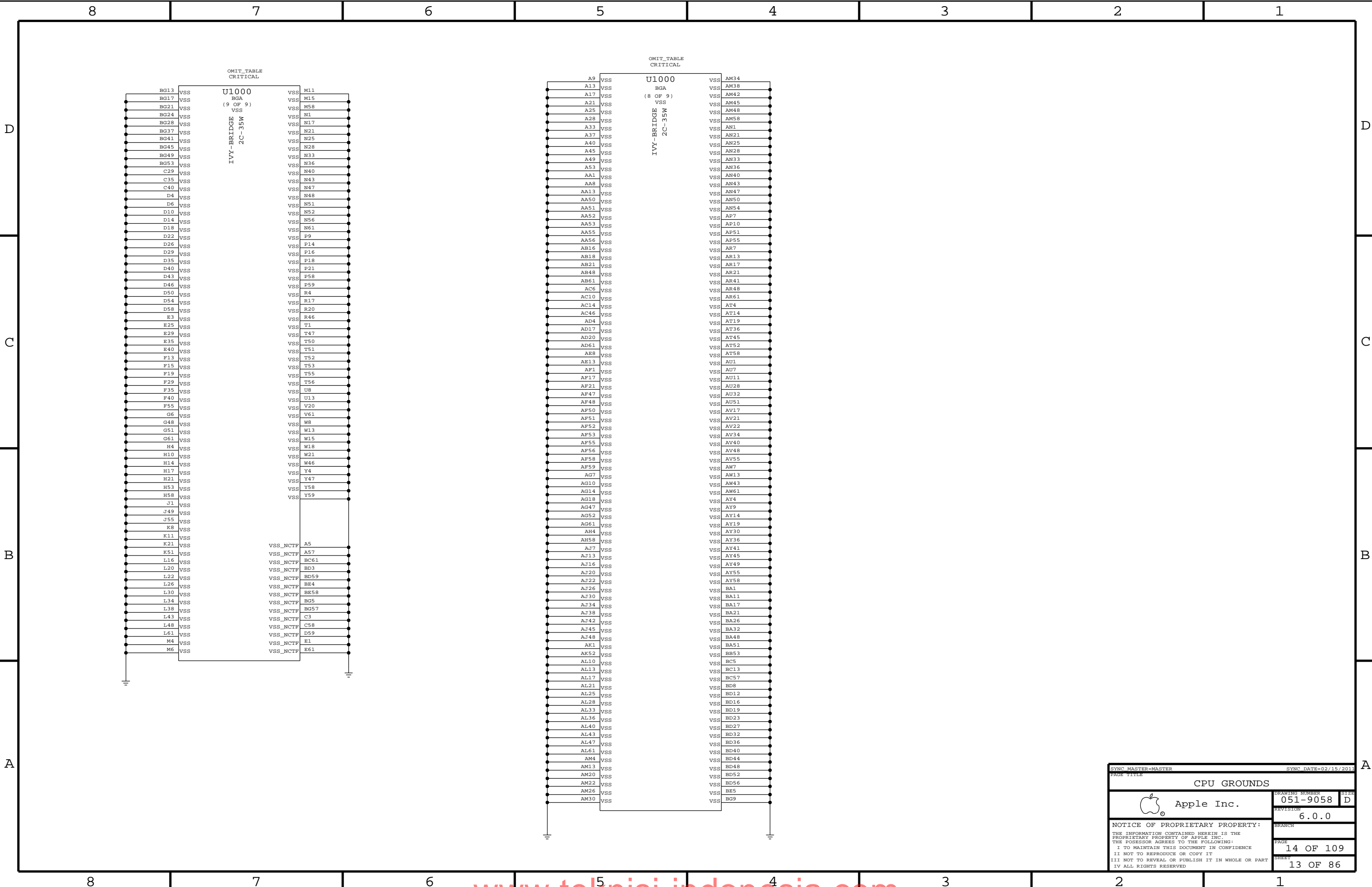









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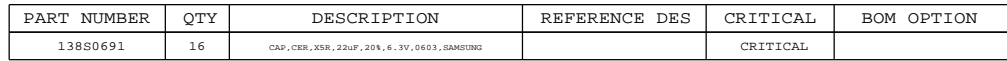
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CPU DECOUPLING-I

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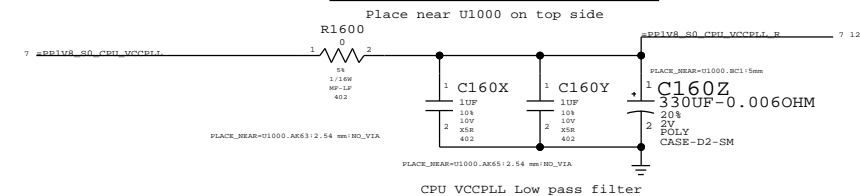


Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

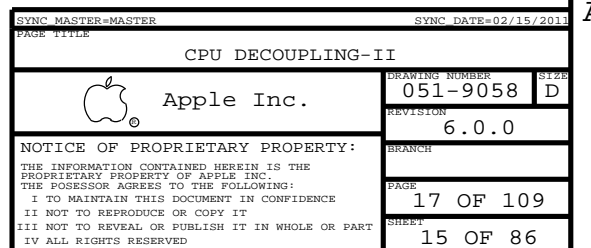
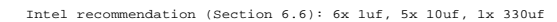
Place near U1000 on top side



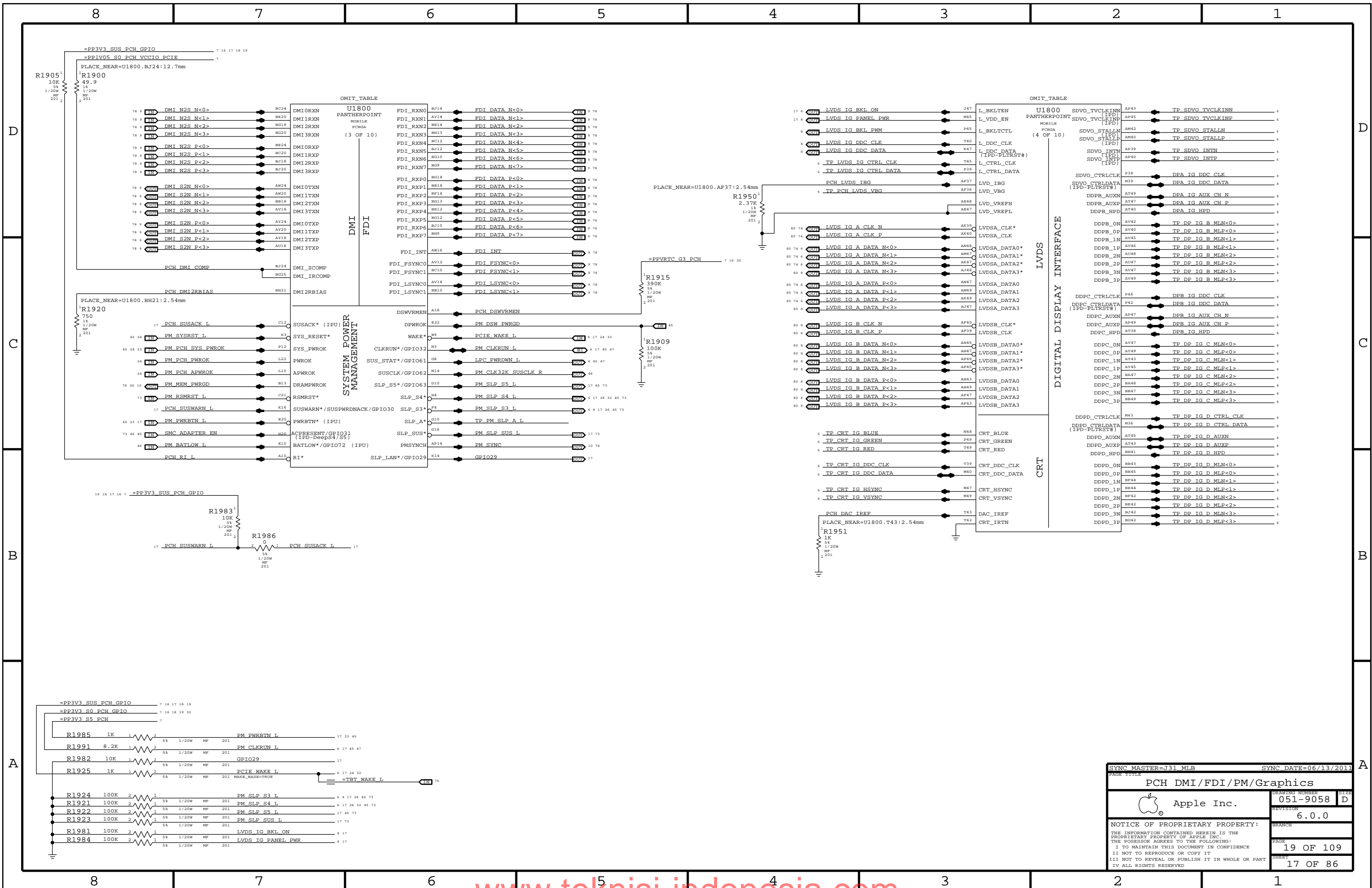
Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF



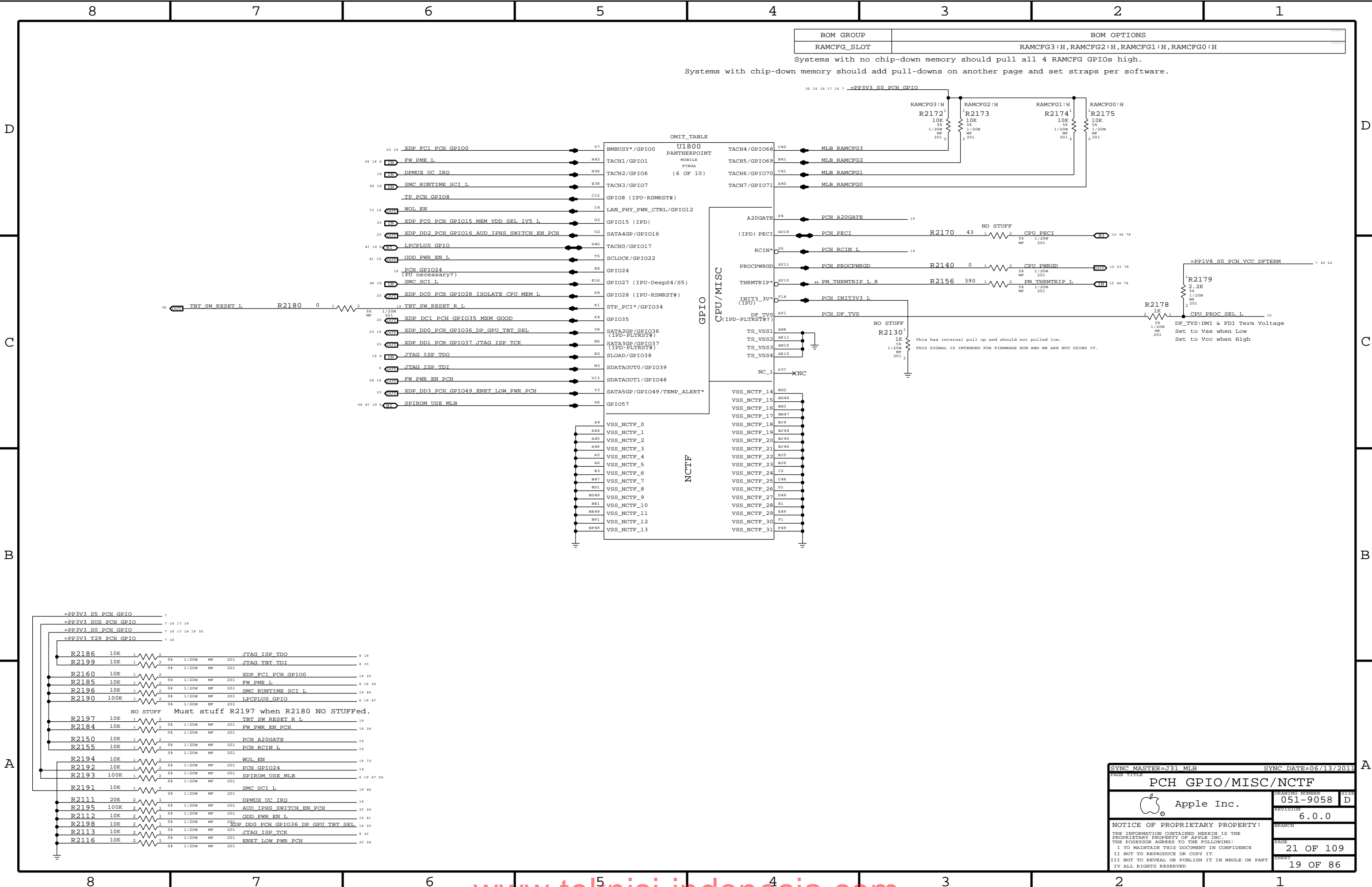
Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF











BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

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PCH GPIO/MISC/NCTF

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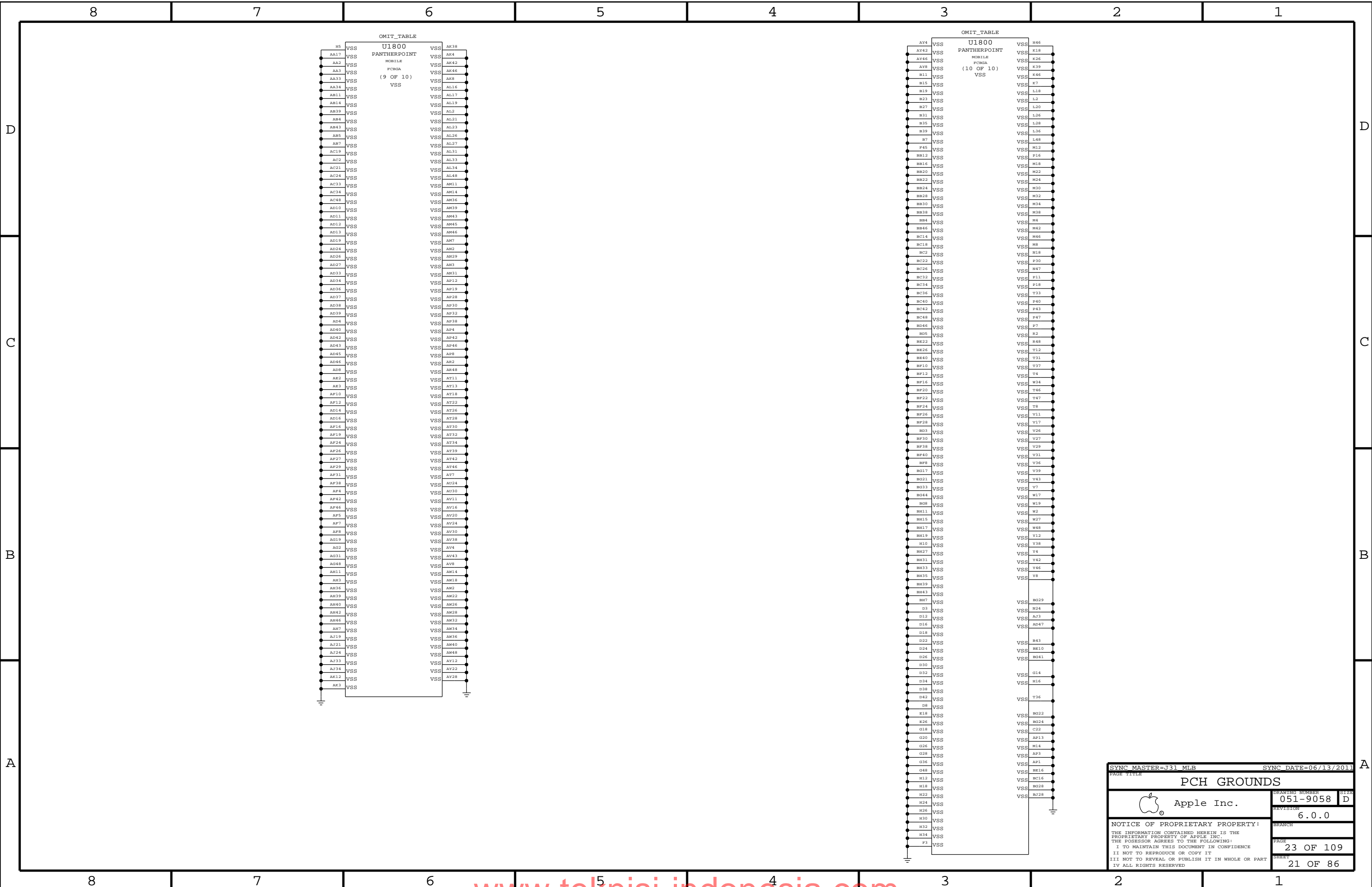
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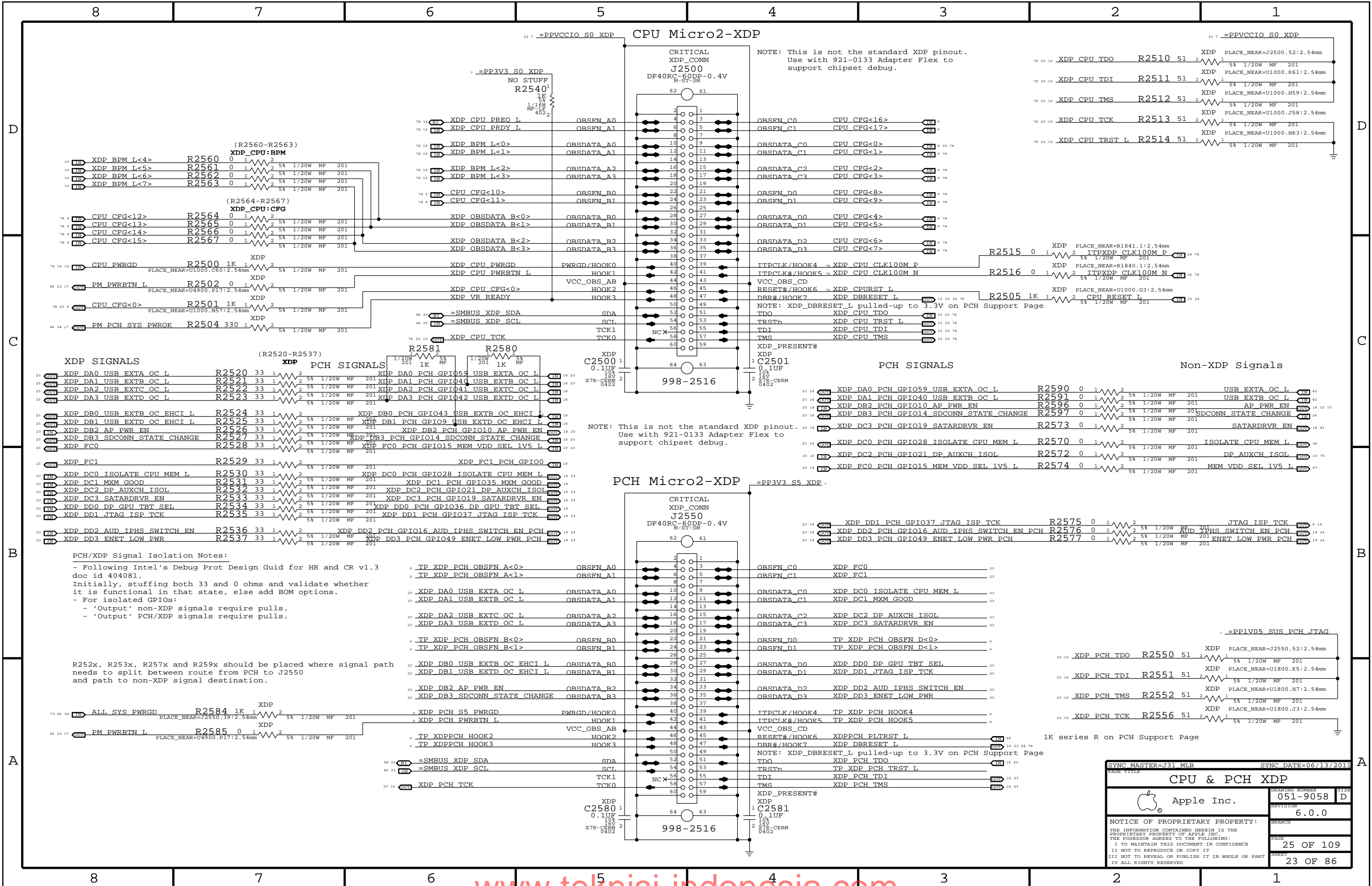
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USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0, HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0, HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1, HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1, HUB_NONREM0_1

NON_REM 1 : NON_REM 0
0 : 0
1 : 1
1 : 1

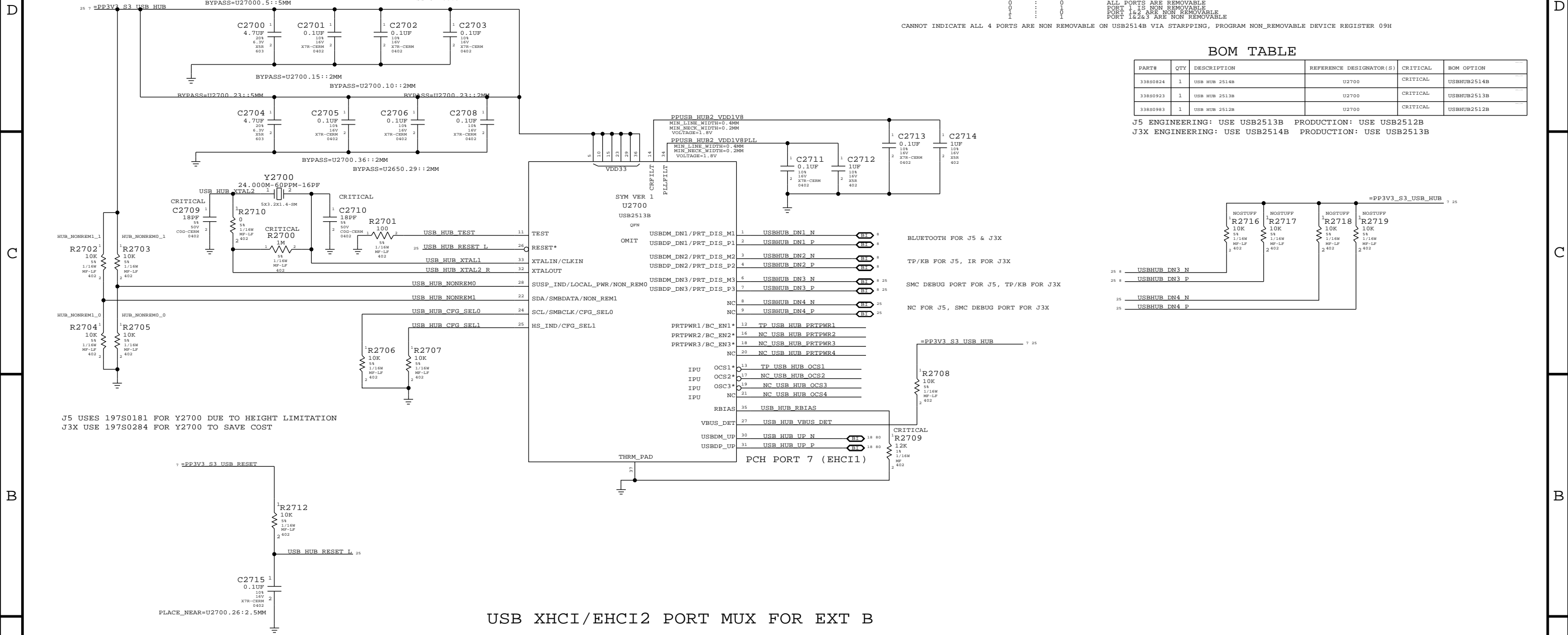
STRAP PIN CFG
ALL PORTS ARE REMOVABLE
PORT 1 IS NON REMOVABLE
PORT 1&2 ARE NON REMOVABLE
PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

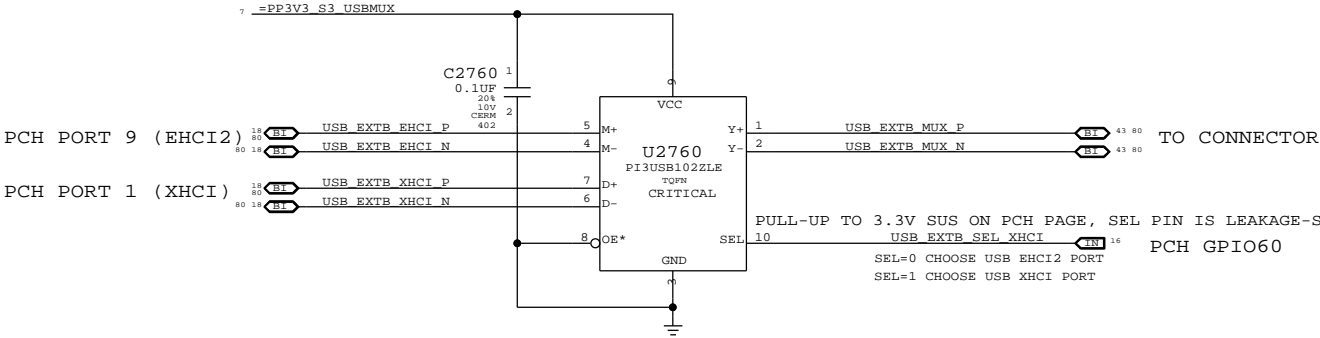
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

J5 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



USB XHCI/EHCI2 PORT MUX FOR EXT B



PAGE TITLE		PAGE NUMBER	
USB HUB & MUX		051-9058	
Apple Inc.		6.0.0	
NOTICE OF PROPRIETARY PROPERTY:		27 OF 109	
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

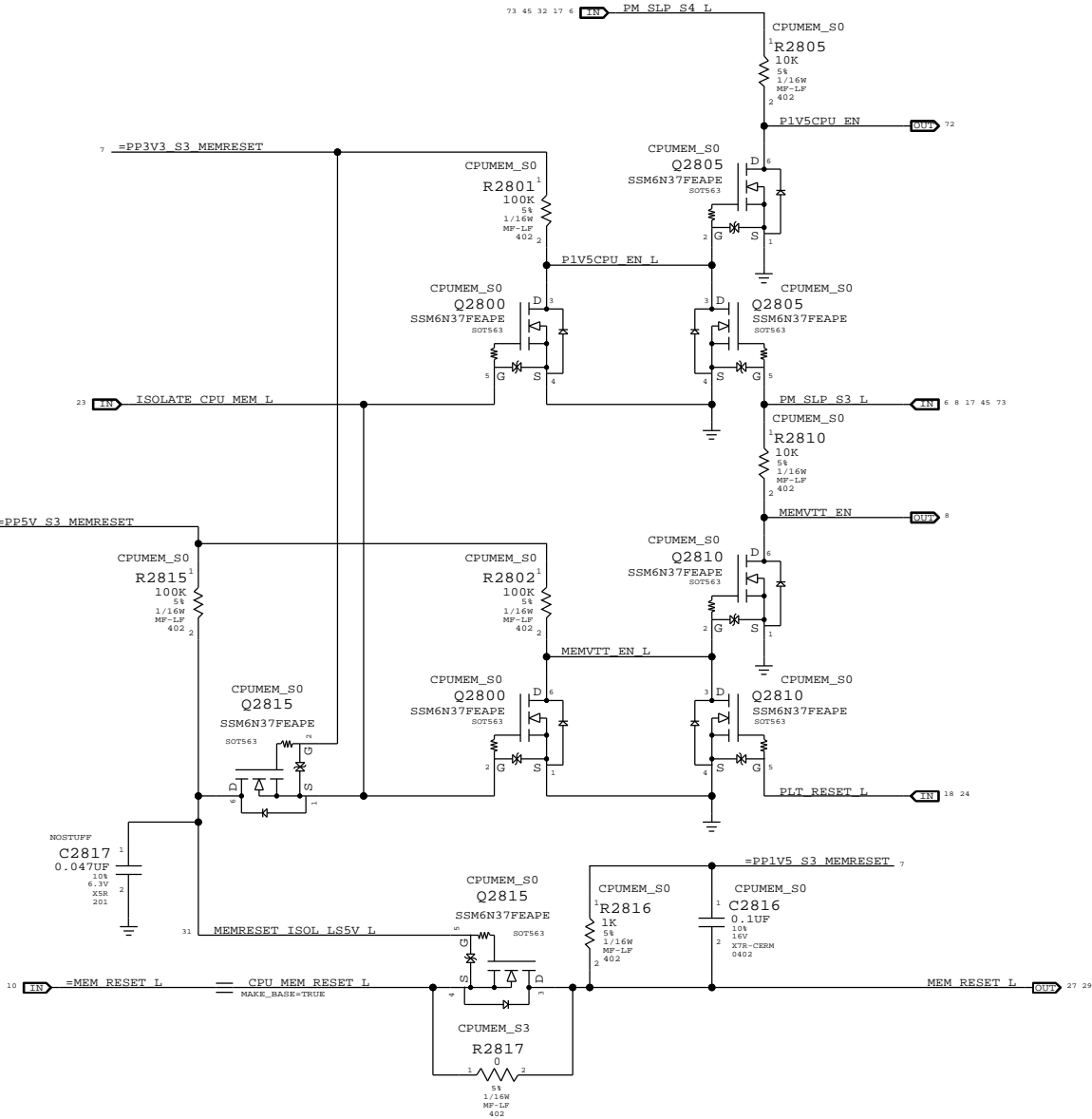
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

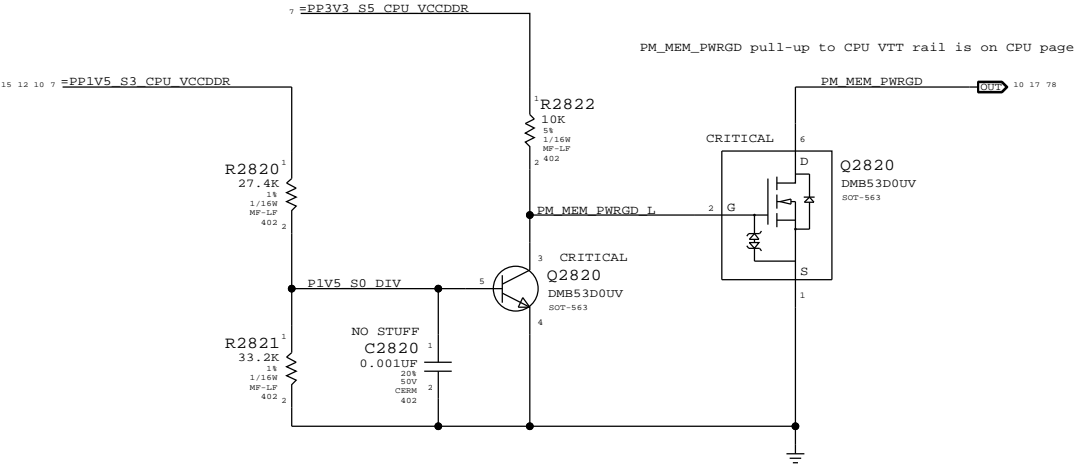
P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

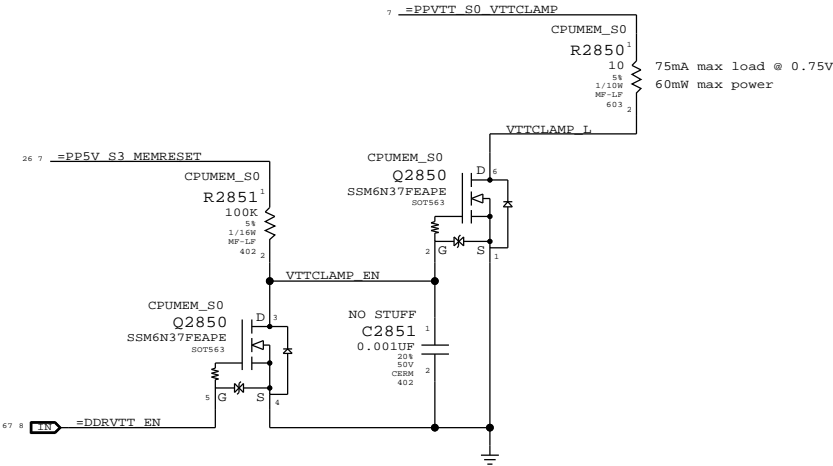


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3

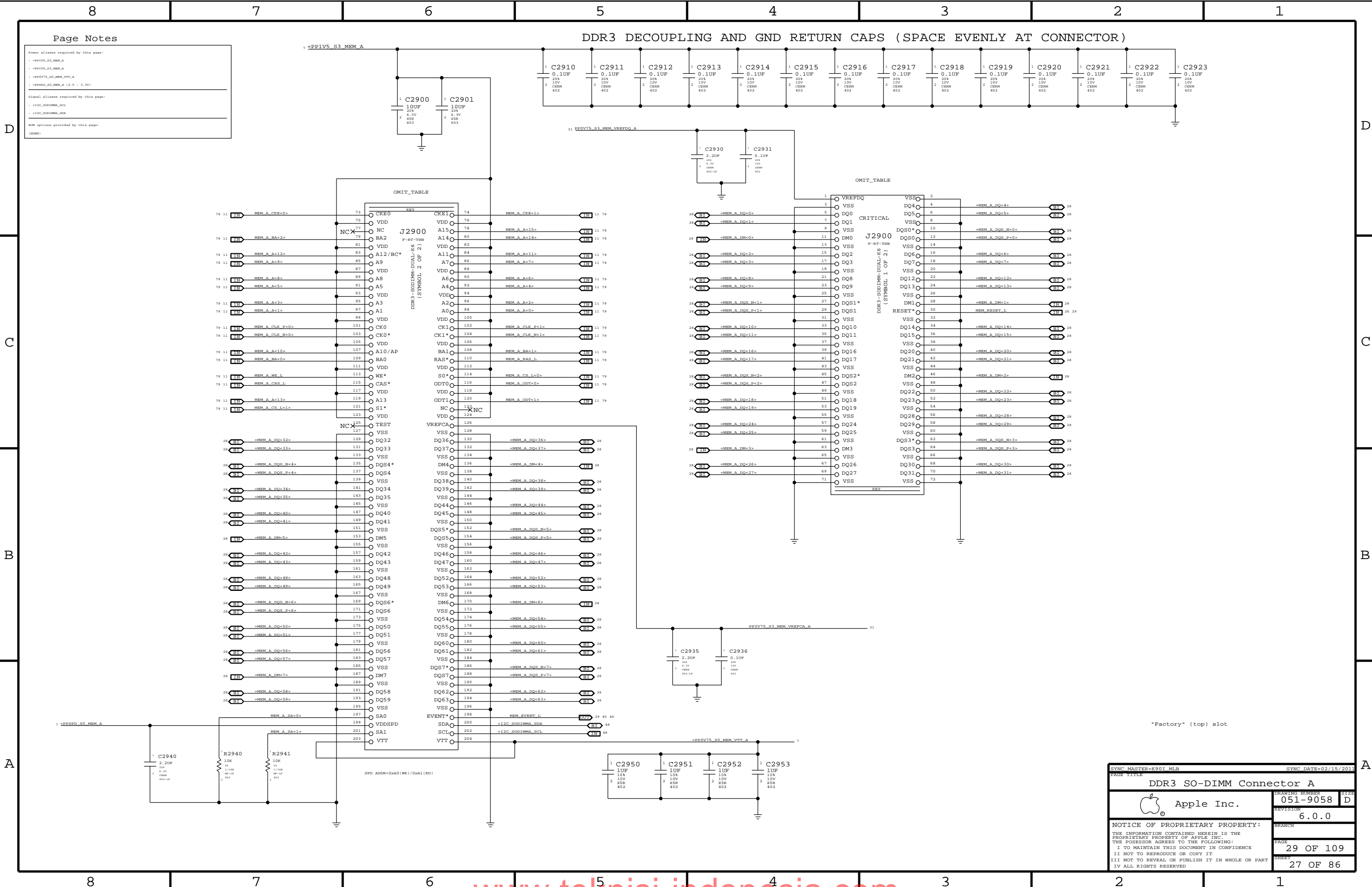


Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
CPU Memory S3 Support			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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Page Notes

Power aliases required by this page:


- PP1V5_S3_MEM_A
- PP1V5_S3_MEM_A
- PP0V75_S3_MEM_VTT_A
- PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- I2C_S0DIMA_SCL
- I2C_S0DIMA_SDA

DOM options provided by this page:

(None)

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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		BRANCH	
		PAGE	29 OF 109
		SHEET	27 OF 86

[illegible]

Page Notes

Power aliases required by this page:
 - >PP1V5_S3_MEM_B
 - >PP1V5_S3_MEM_B
 - >PP0V75_S3_MEM_VTT_B
 - >PPSPD_S0_MEM_B (2.5 - 3.3V)
 Signal aliases required by this page:
 - >I2C_S0D1MMB_SCL
 - >I2C_S0D1MMB_SDA
 ROM options provided by this page:
 (None)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

D

D

C

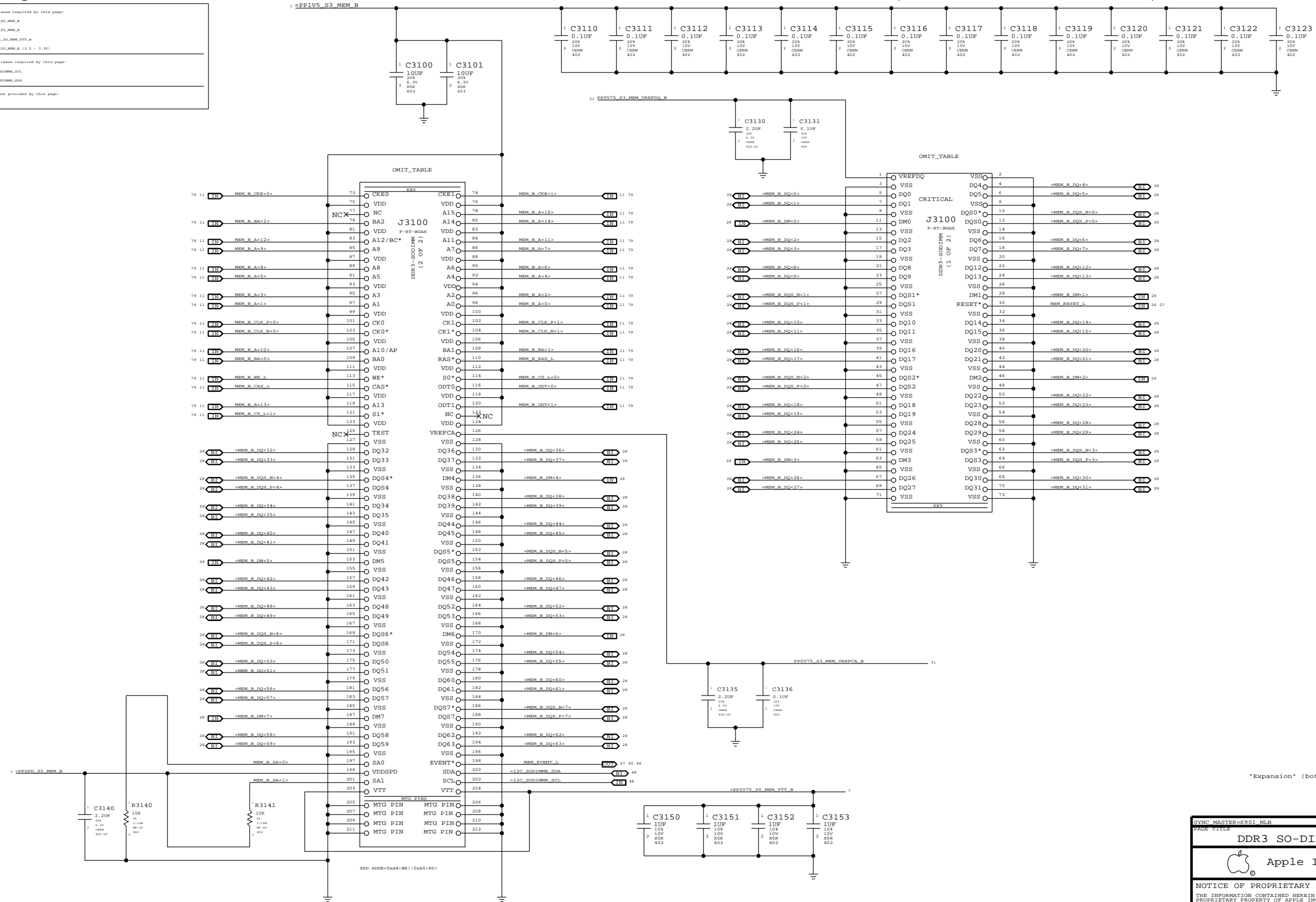
C

B

B

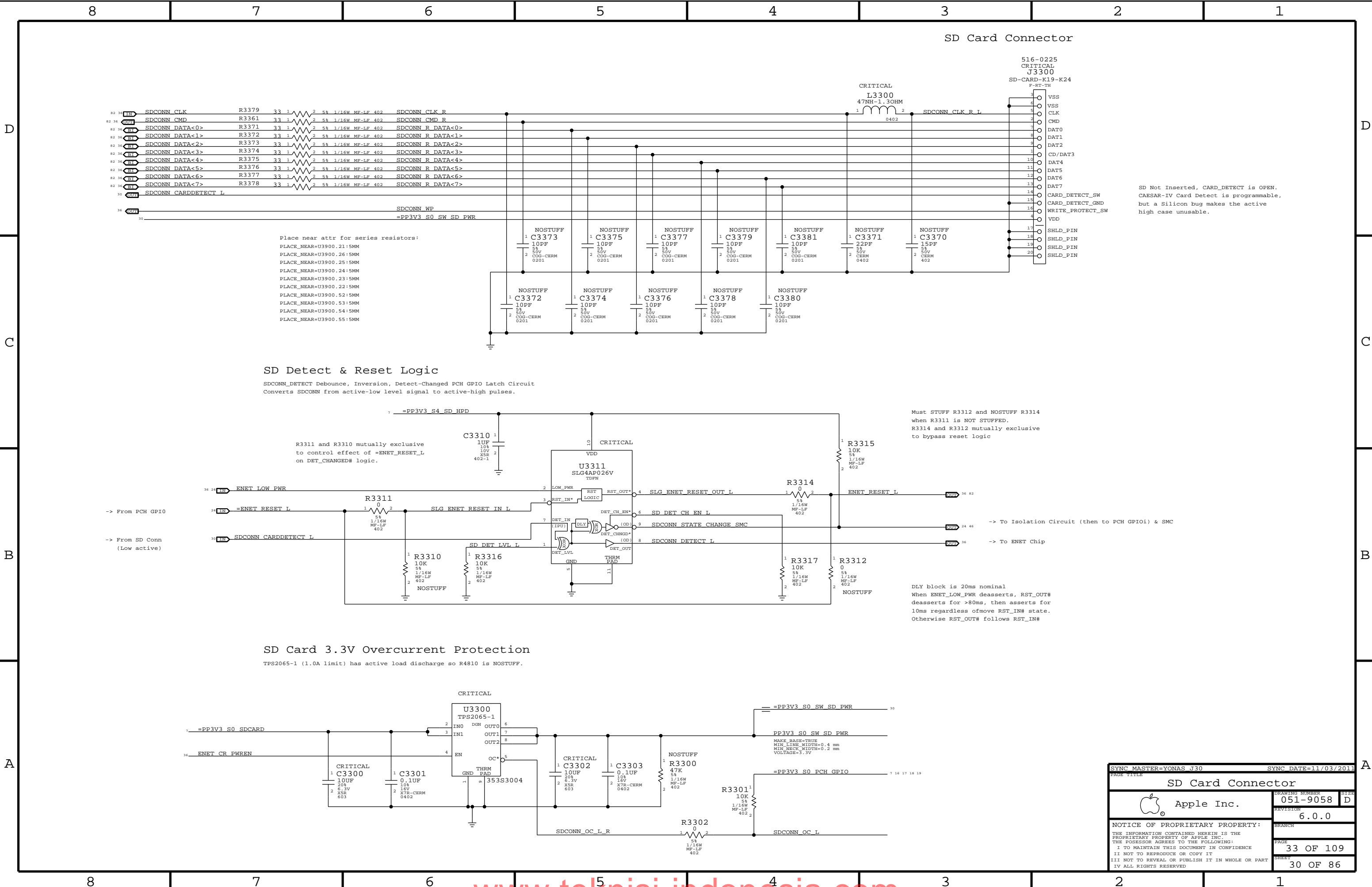
A

A



"Expansion" (bottom) slot

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
DDR3 SO-DIMM Connector B			
Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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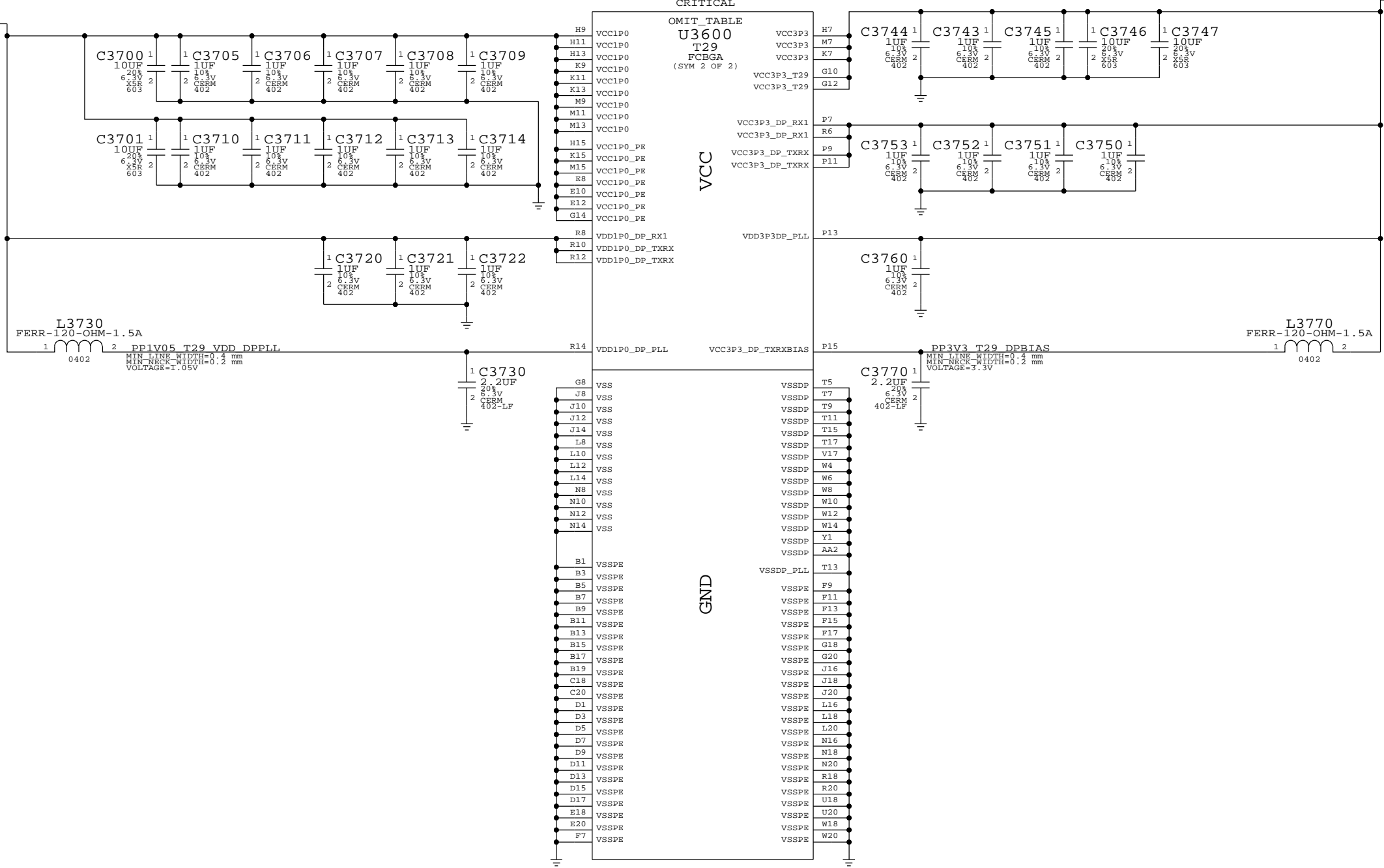
D
C
B
A

D
C
B
A

8 7 6 5 4 3 2 1

=PP1V05 T29_RTR
2100 mA (Single Port)
2250 mA (Dual Port)
EDP: 3000 mA

=PP3V3 T29_RTR 7 33 35
135 mA (Single-Port)
152 mA (Dual-Port)
EDP: 200 mA



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
T29 Host (2 of 2)			
		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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		PAGE	37 OF 109
		SHEET	34 OF 86

8 7 6 5 4 3 2 1

Page Notes

Power aliases required by this page:

- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL (3.3V FET Input)
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

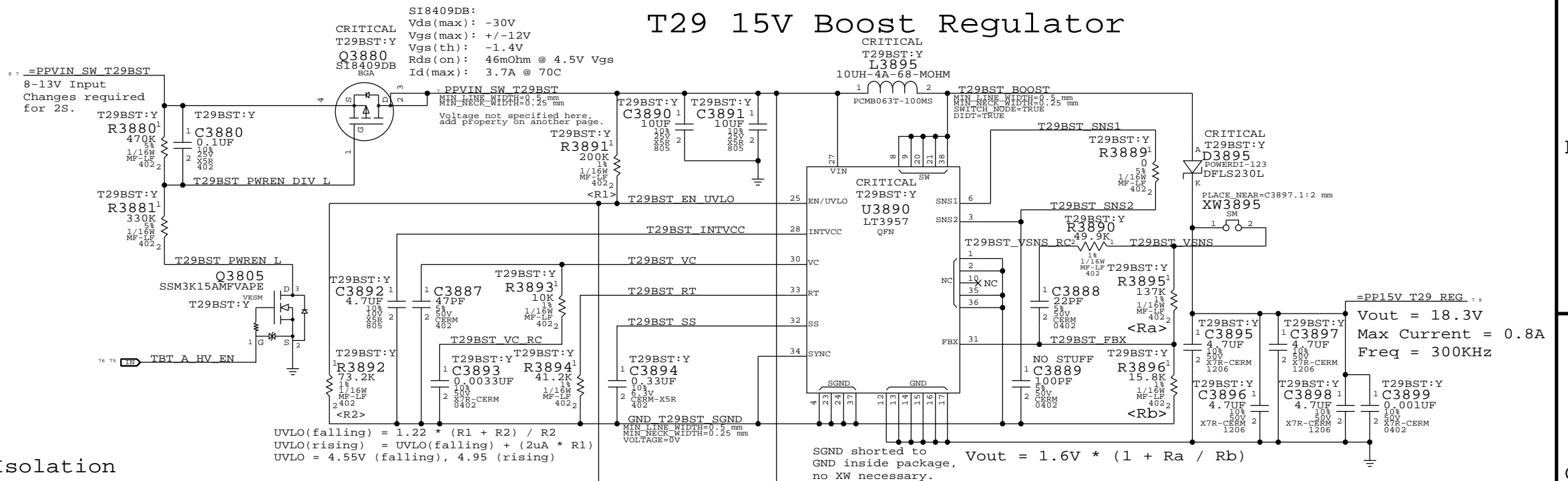
Signal aliases required by this page:

- =T29_CLKREQ_L
- =T29_RESET_L

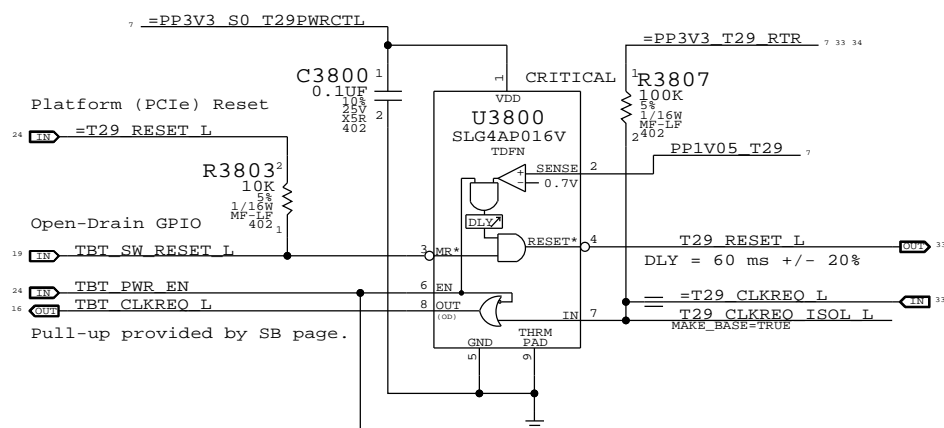
BOM options provided by this page:

T29BST:Y - Stuffs 18V boost circuitry.

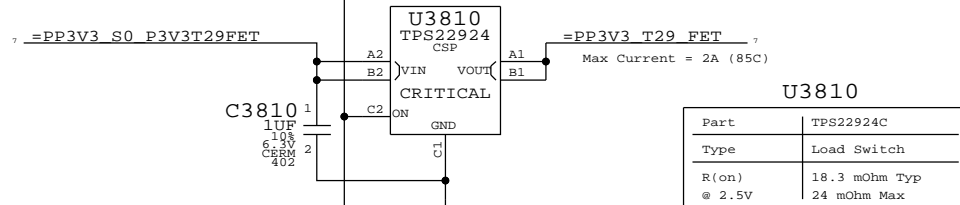
T29 15V Boost Regulator



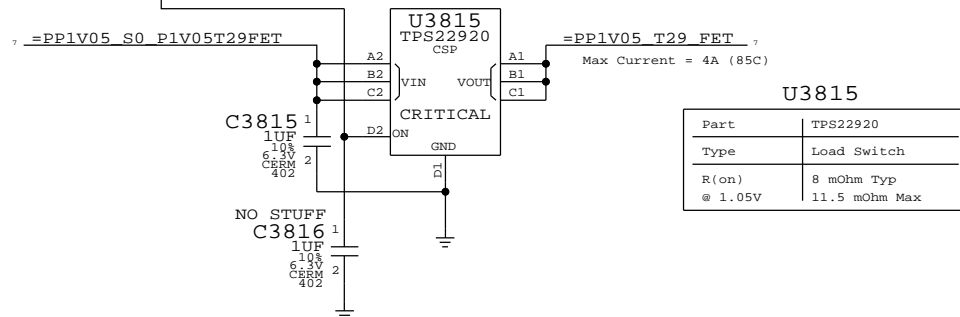
Supervisor & CLKREQ# Isolation




3.3V T29 Switch



1.05V T29 Switch



SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
T29 Power Support			
	Apple Inc.	DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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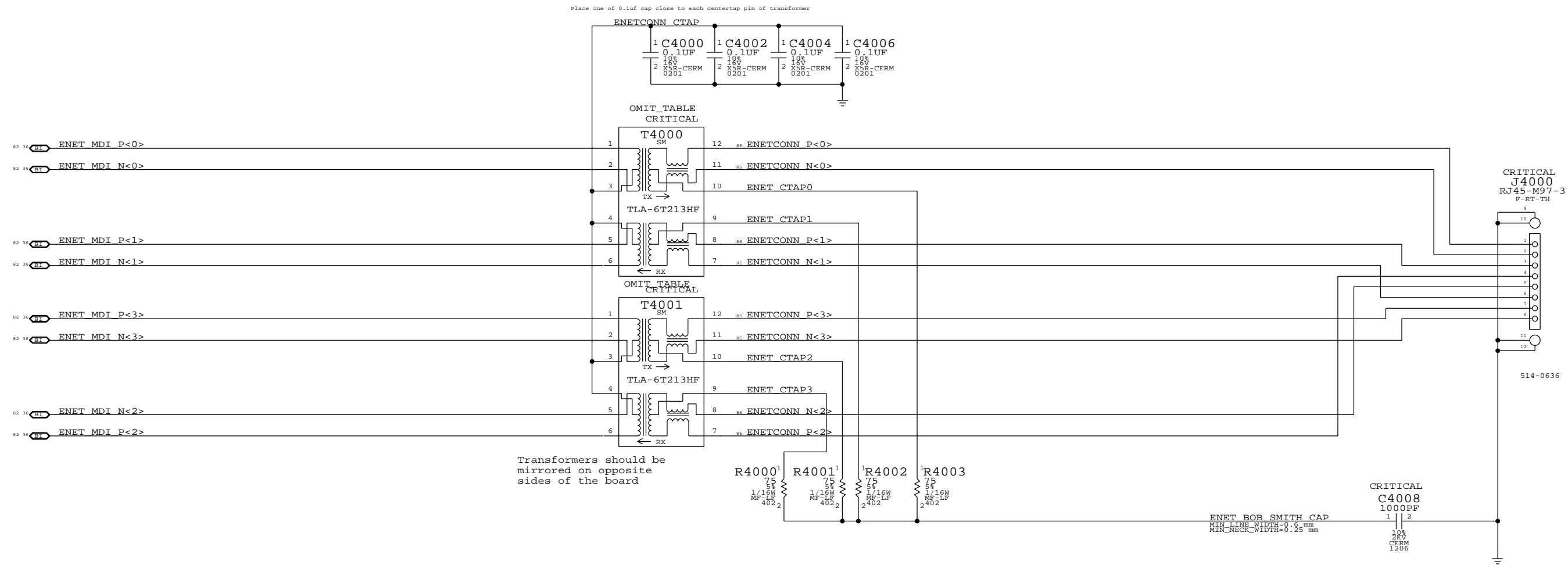


Page Notes


Power aliases required by this page:
(NONE)

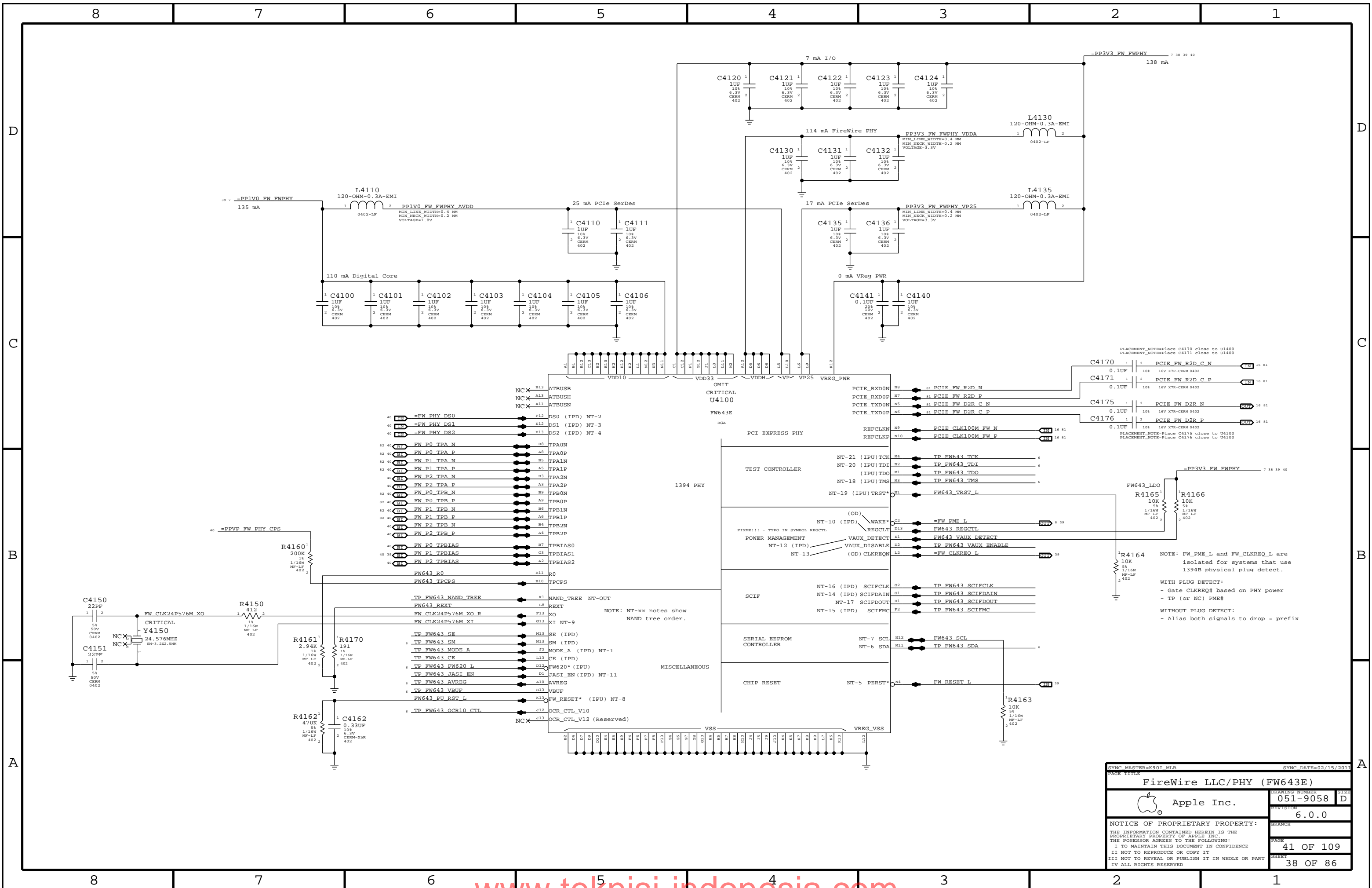
Signal aliases required by this page:
(NONE)


BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
157S0084	2	XFMR, ISO, HALF-PORT, 1000T, 12P, SMD, HF	T4000, T4001	CRITICAL	

SYNC MASTER=K901 MLB		SYNC DATE=02/15/2013	
PAGE TITLE			
Ethernet Connector			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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		PAGE	40 OF 109
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SYNC MASTER=K901 MLR		SYNC DATE=02/15/2011	
PAGE TITLE			
FireWire LLC/PHY (FW643E)			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

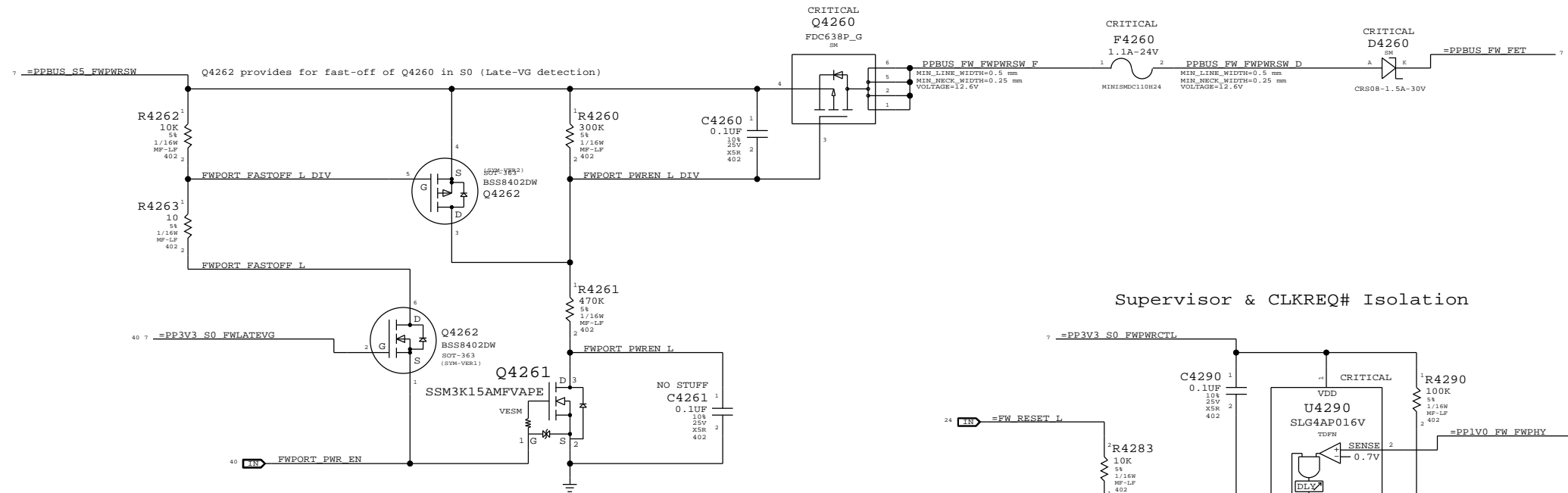
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

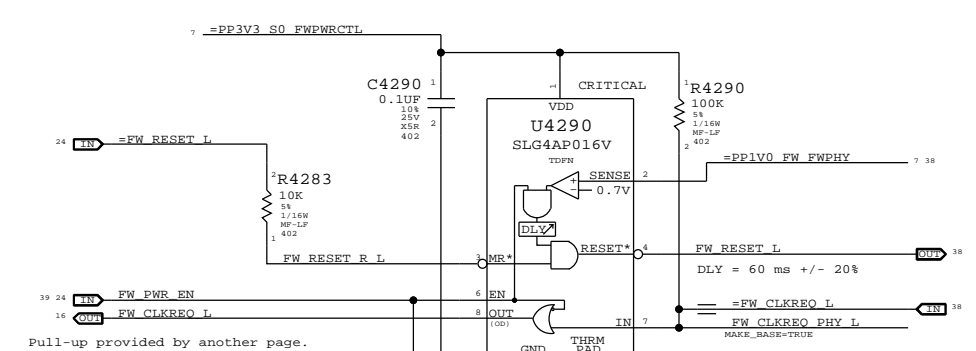
BOM options provided by this page:

(NONE)

FireWire Port Power Switch

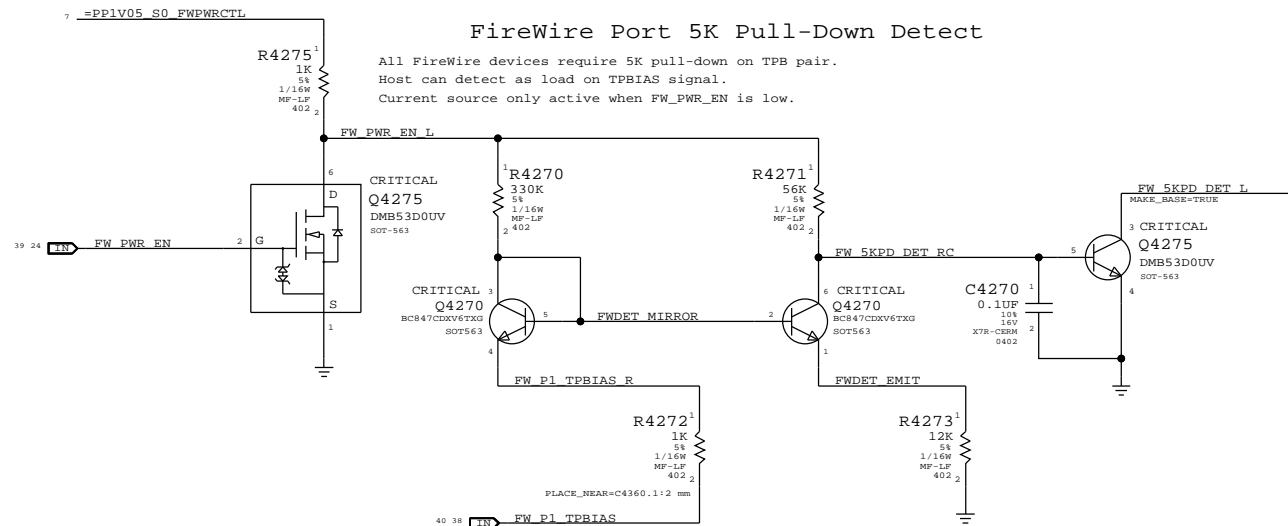


Supervisor & CLKREQ# Isolation



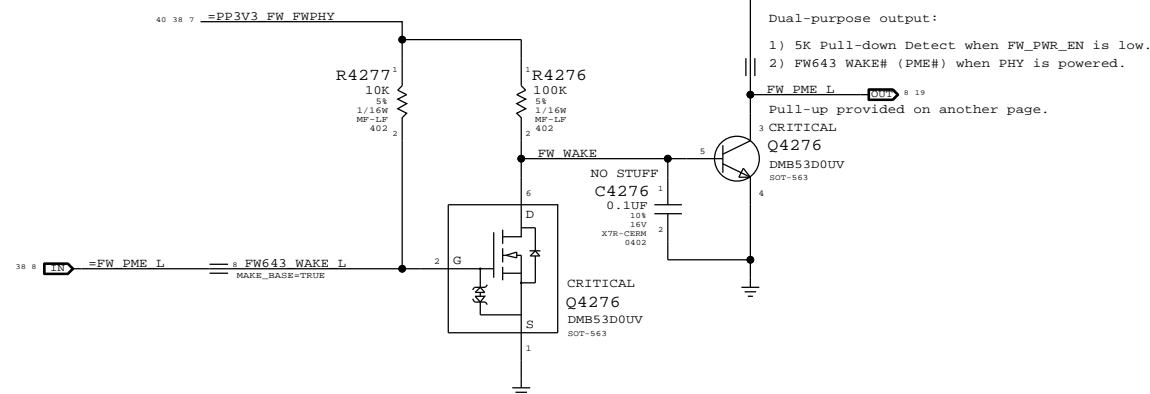
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

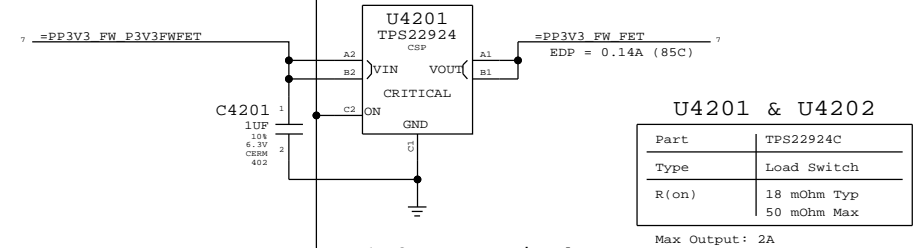


FireWire PHY WAKE# Support

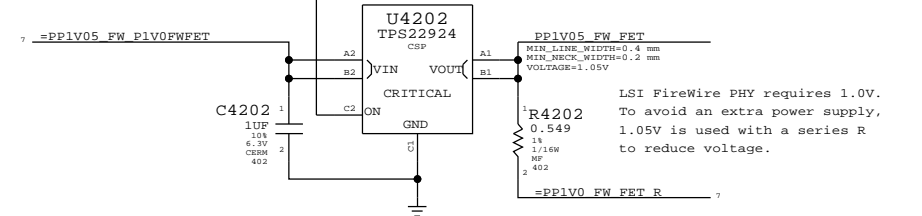
When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.




3.3V FW Switch



1.0V FW Switch



TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=K901 MLB		SYNC DATE=06/23/2011	
PAGE TITLE			
FireWire Port & PHY Power			
	Apple Inc.	DRAWING NUMBER	051-9058
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		REVISION	6.0.0
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

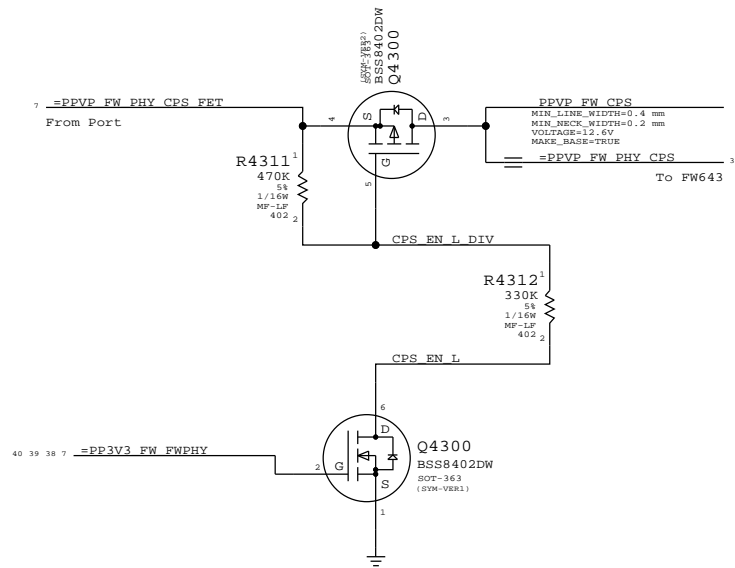
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

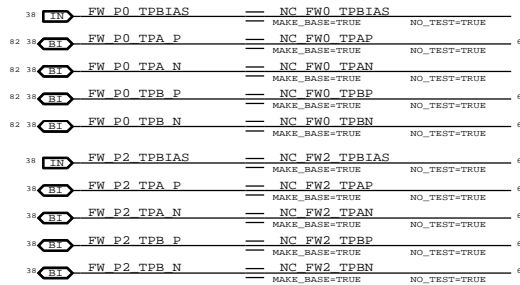
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



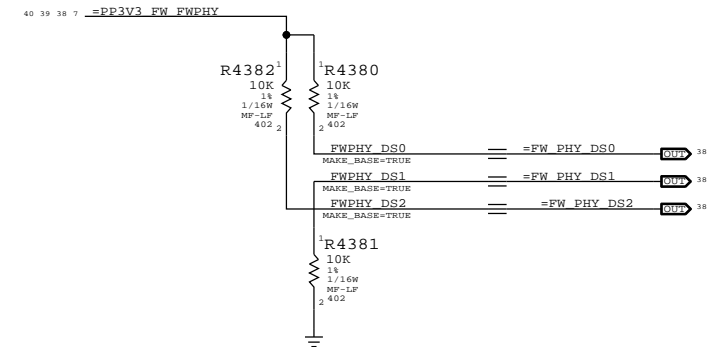
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



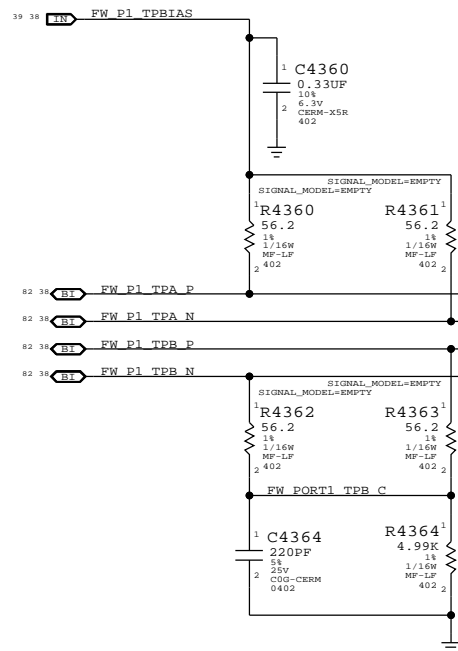
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)



Termination

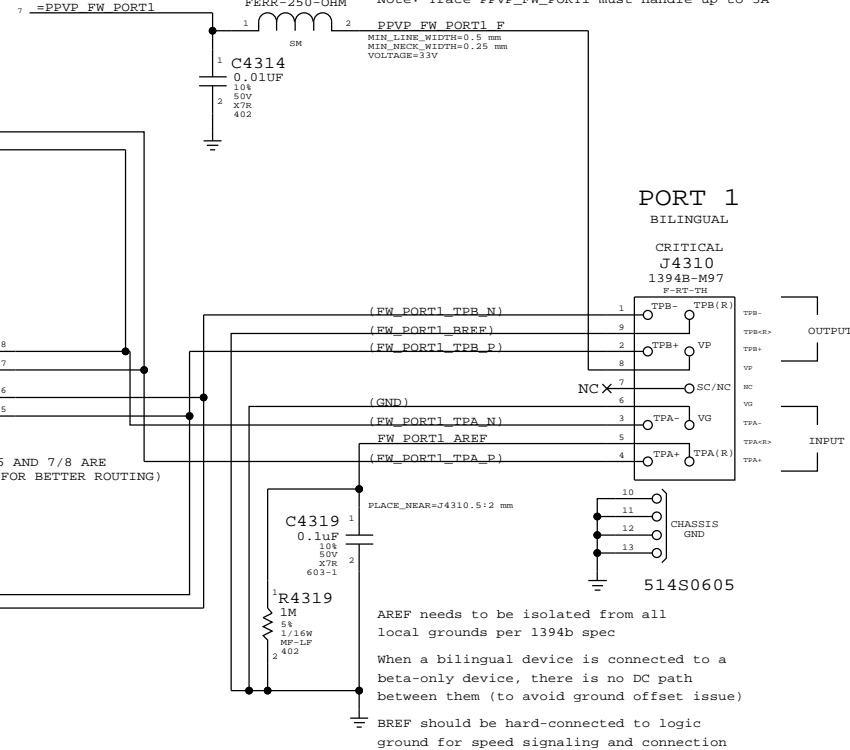
Place close to FireWire PHY



Cable Power

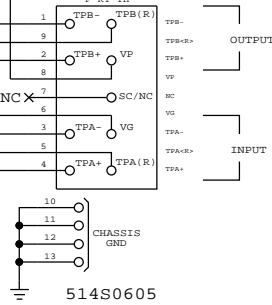
CRITICAL
L4310
FERR-250-OHM

Note: Trace PPVP_FW_PORT1 must handle up to 5A




PORT 1 BILINGUAL

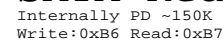
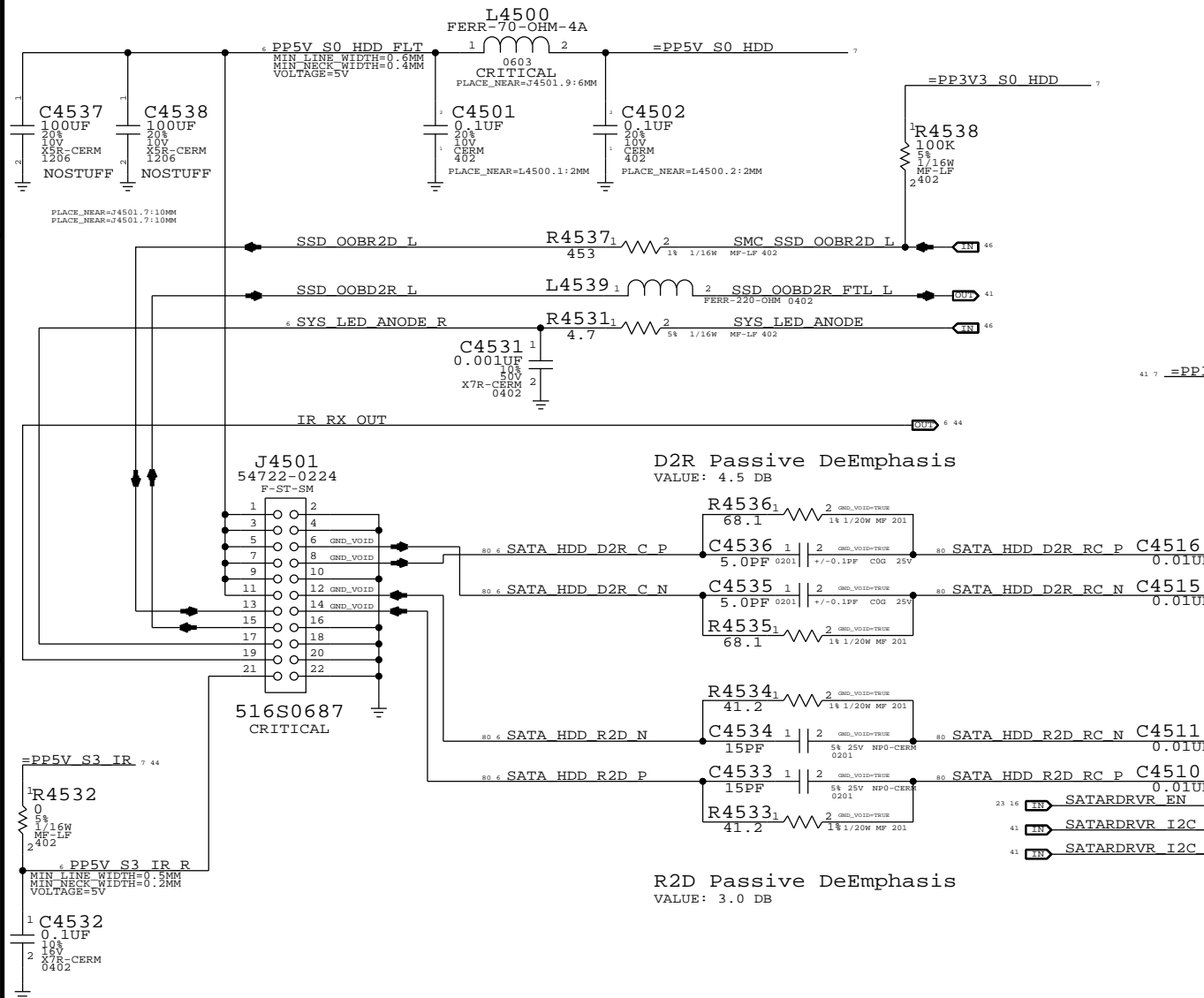
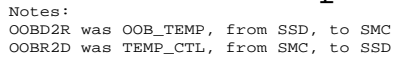
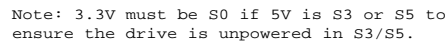
CRITICAL
J4310
1394B-M97
F-RT-TH



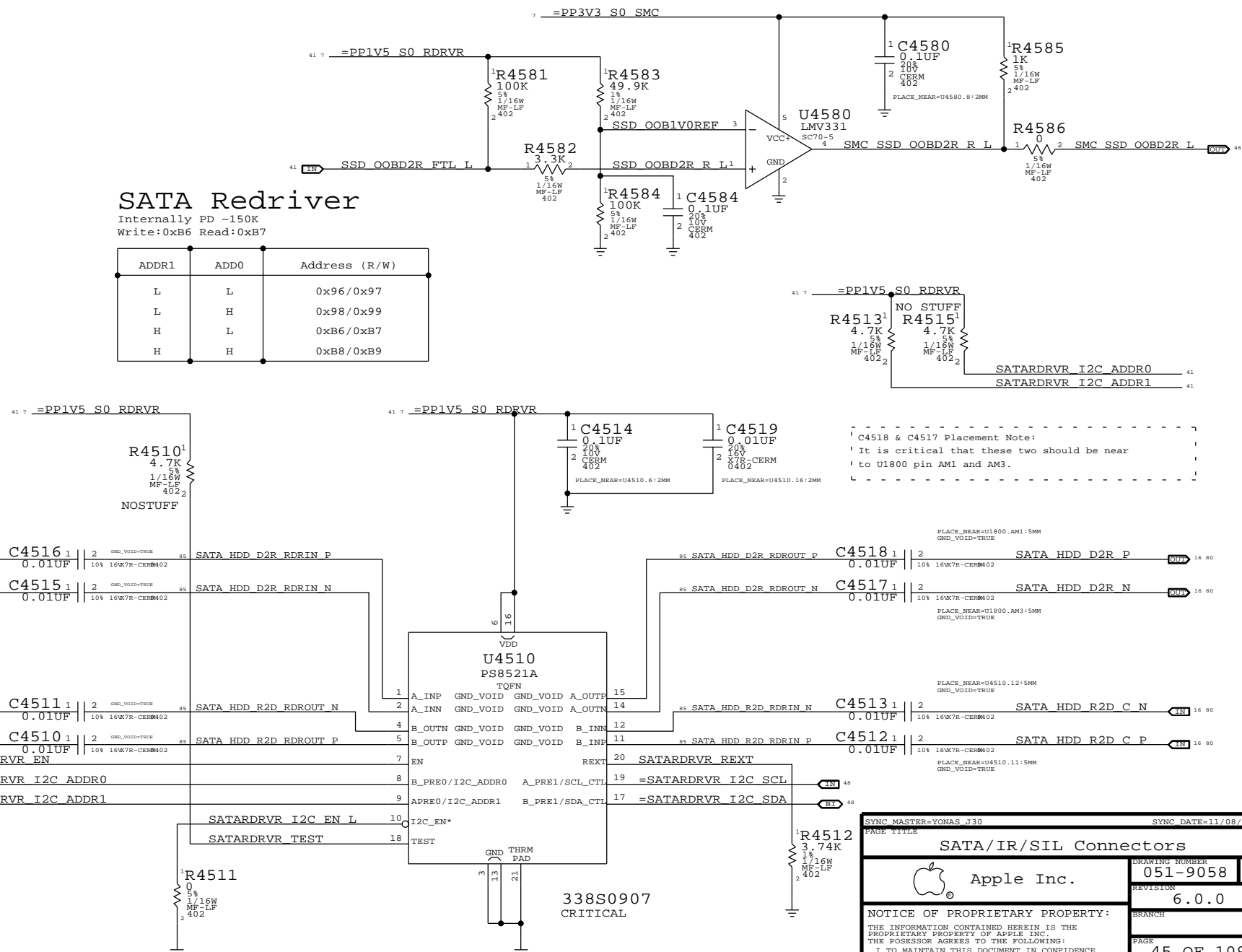
AREF needs to be isolated from all local grounds per 1394b spec
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)
BREF should be hard-connected to logic ground for speed signaling and connection


CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

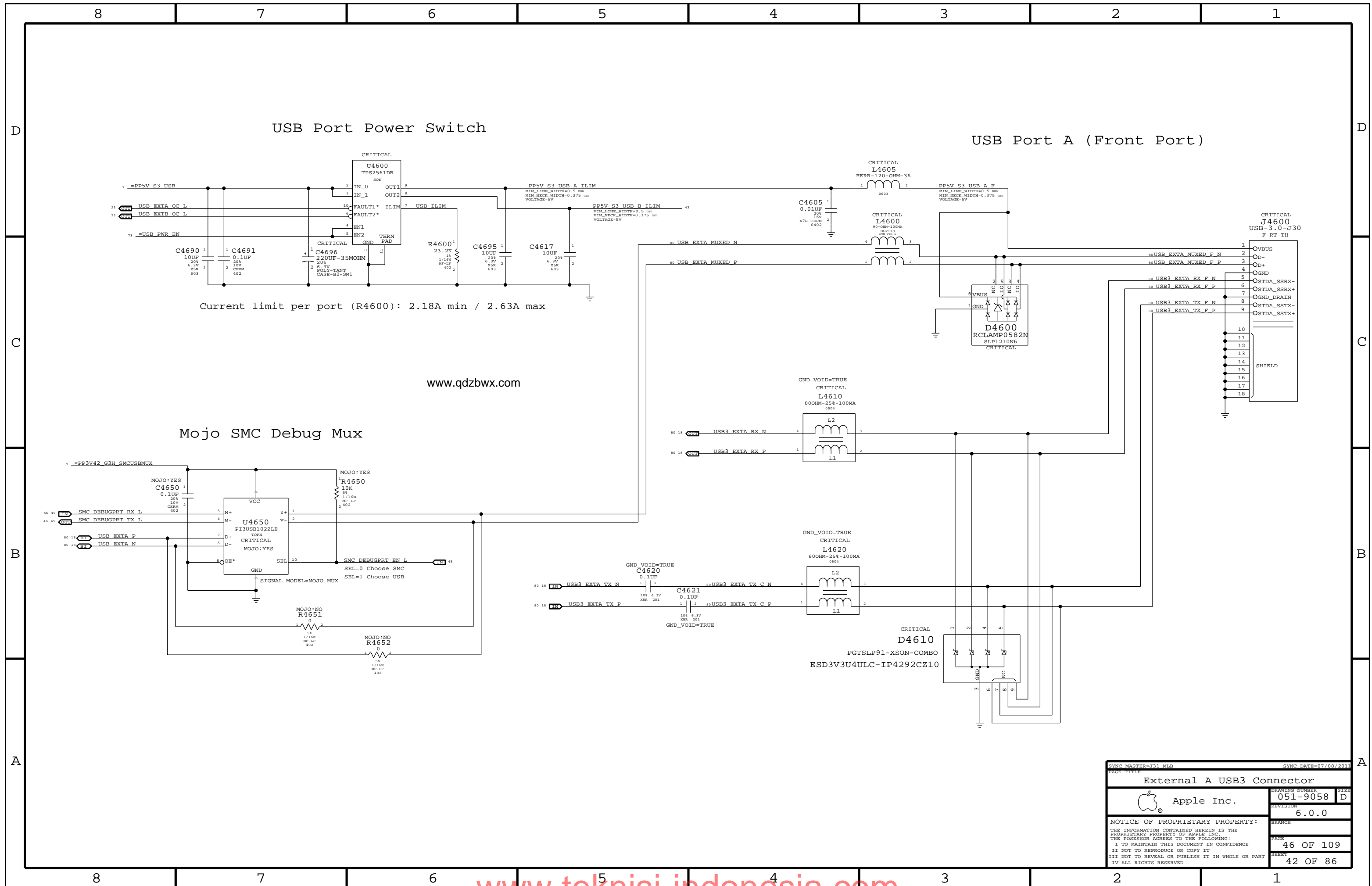
SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
FireWire Connector			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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
ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

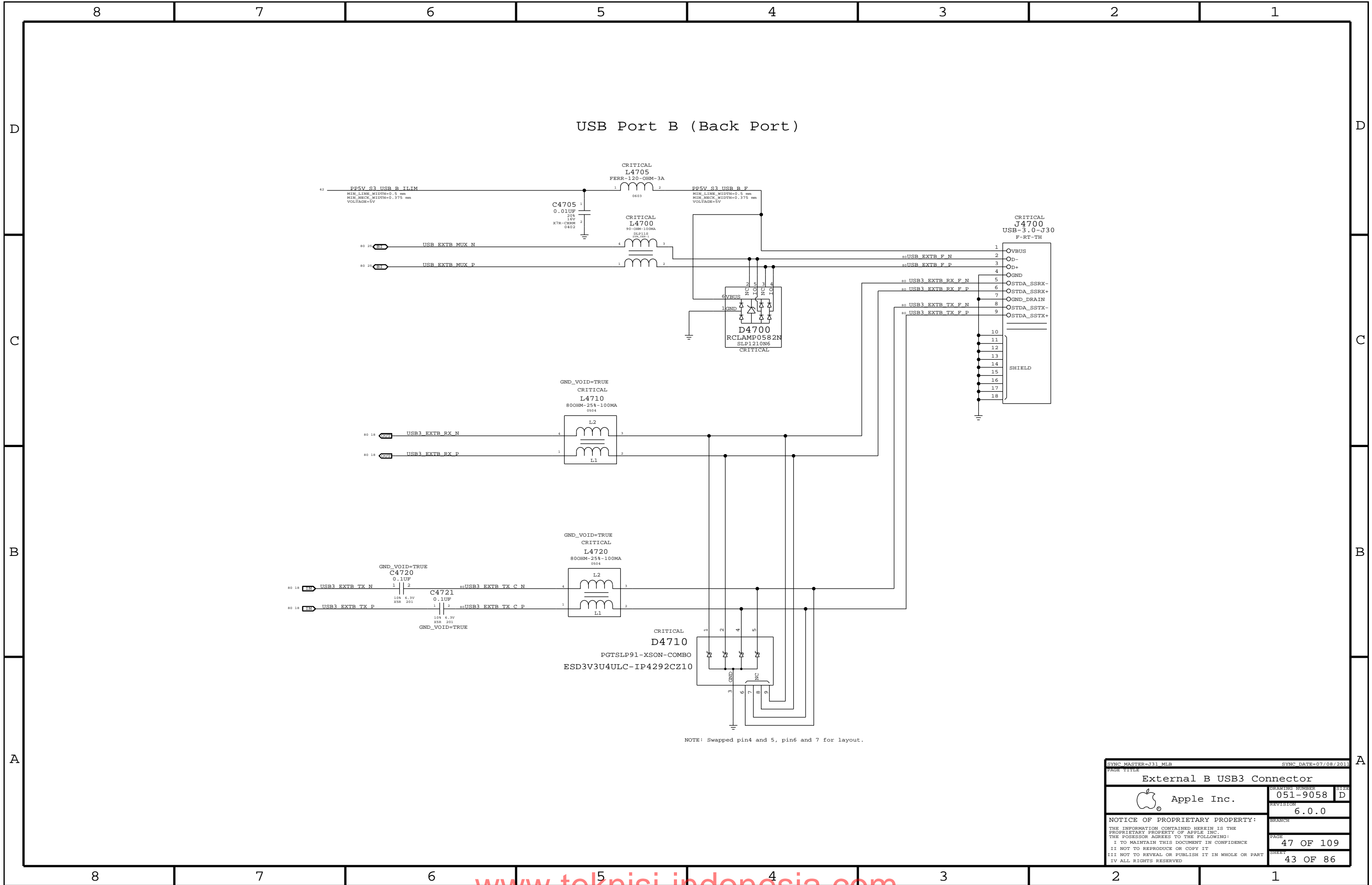



2		SYNC MASTER=TONAS J30 SYNC DATE=11/08/2011	
PAGE TITLE		SATA/IR/SIL Connectors	
 Apple Inc.		DRAWING NUMBER 051-9058	SIZE D
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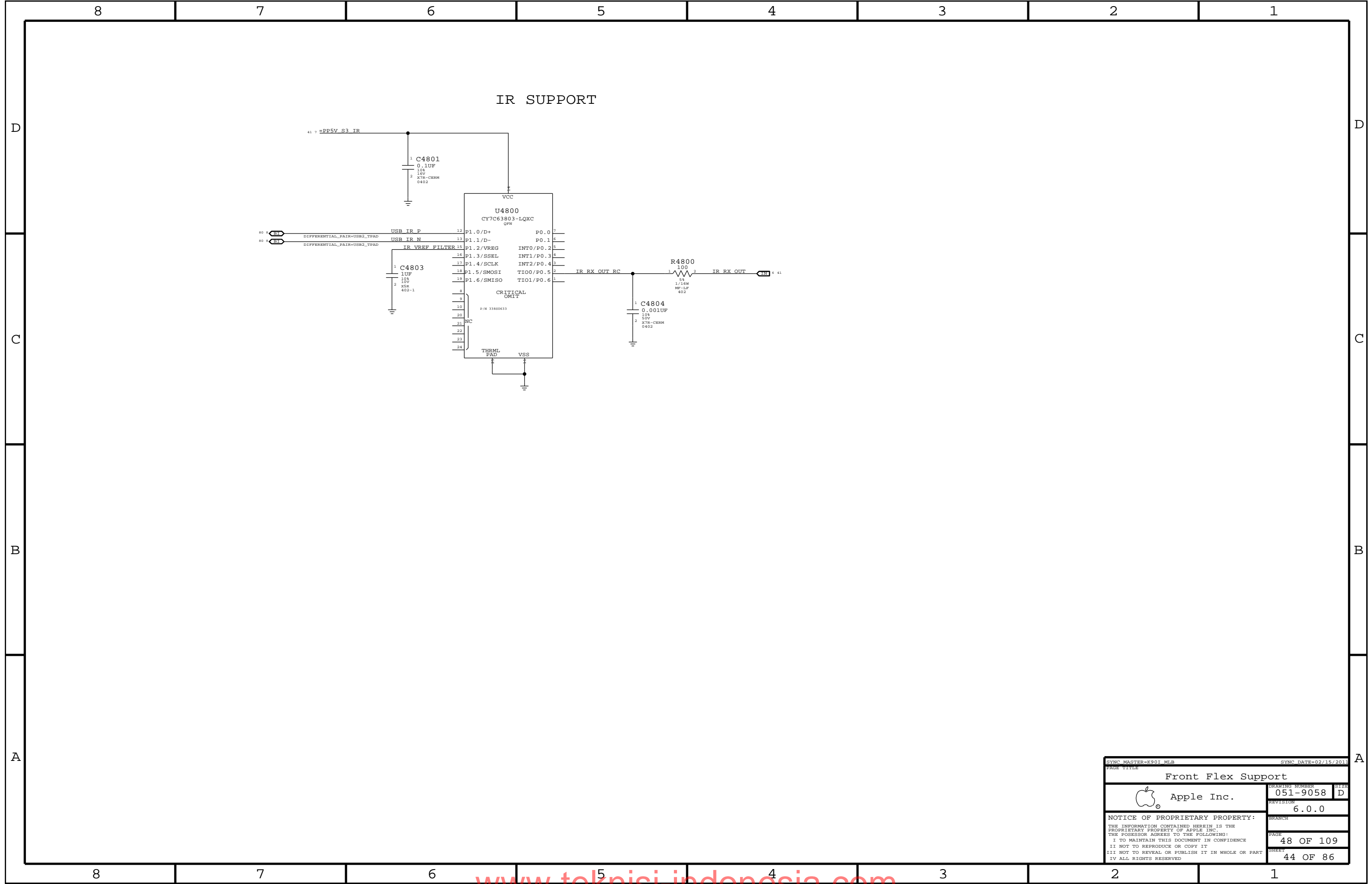


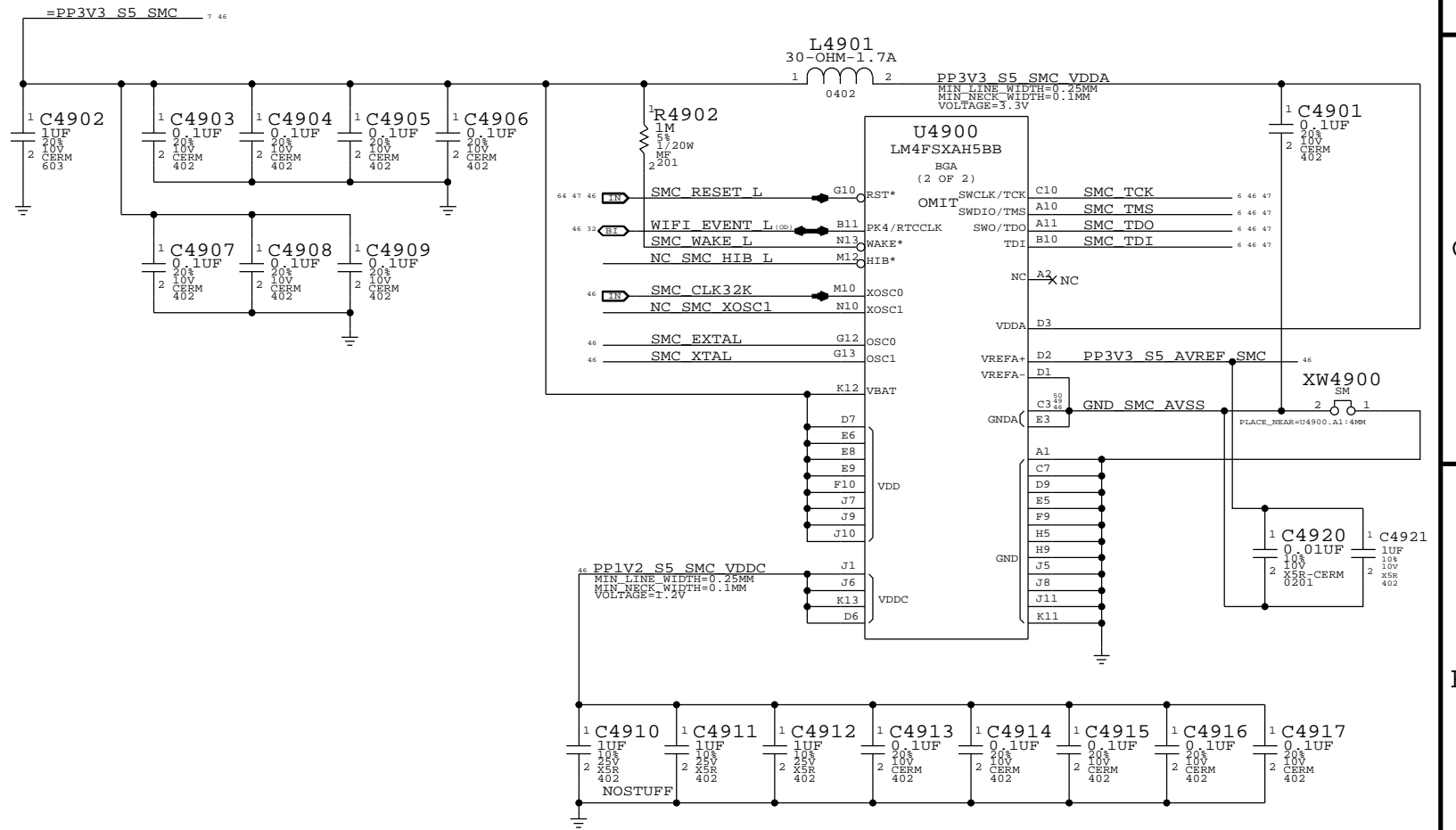
www.qdzbwx.com


SYNC MASTER=J31 MLB		SYNC DATE=07/08/2011	
PAGE TITLE			
External A USB3 Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9058		D
	REVISION		
		6.0.0	
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SYNC MASTER=J31 MLB		SYNC DATE=07/08/2013	
PAGE TITLE			
External B USB3 Connector			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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SYNC MASTER=YOMAS J30		SYNC DATE=12/21/2011	
PAGE TITLE			
SMC			
 Apple Inc.		DRAWING NUMBER 051-9058	
		SIZE D	
		REVISION 6.0.0	
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		SHEET 45 OF 86	

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



C |



B

B



B

A



A



PM CLK32K SUSCLK R1 22 SMC CLK32K
PLACE NEAR=U1800.N14:5MM 5% 1/20W MF 201

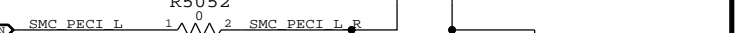
1/16W
MF-LF
402



SMCBATLOW =PP3V3

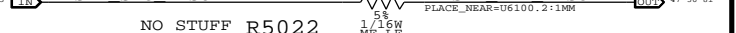


2	1
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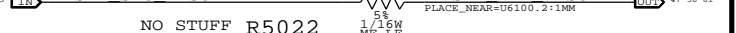


NO STUFF R5022 1/16W 5% PLACE_NEAR=U6100.2:1MM

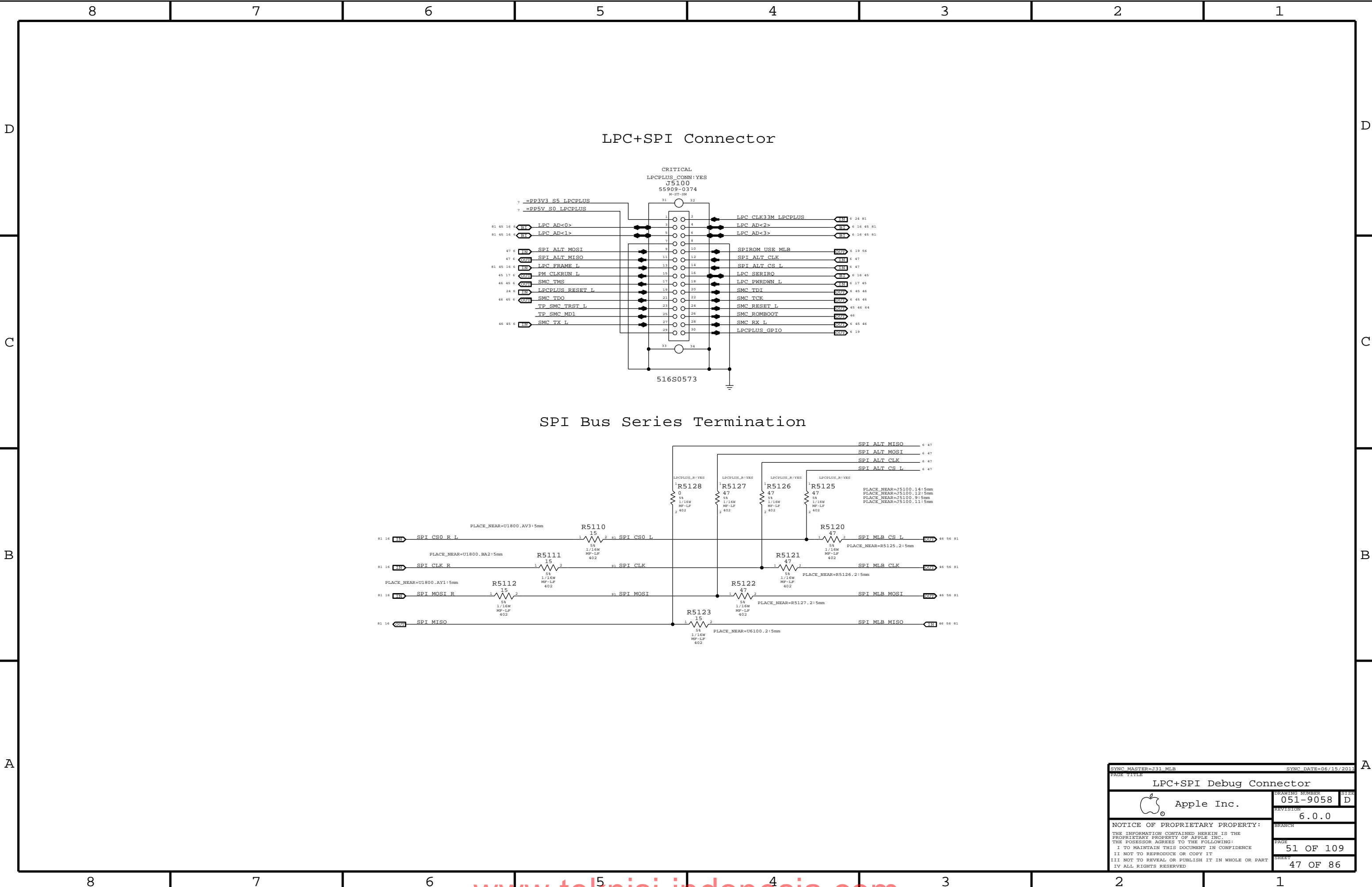
NO STUFF R5022 1/16W 5% PLACE_NEAR=U6100.2:1MM

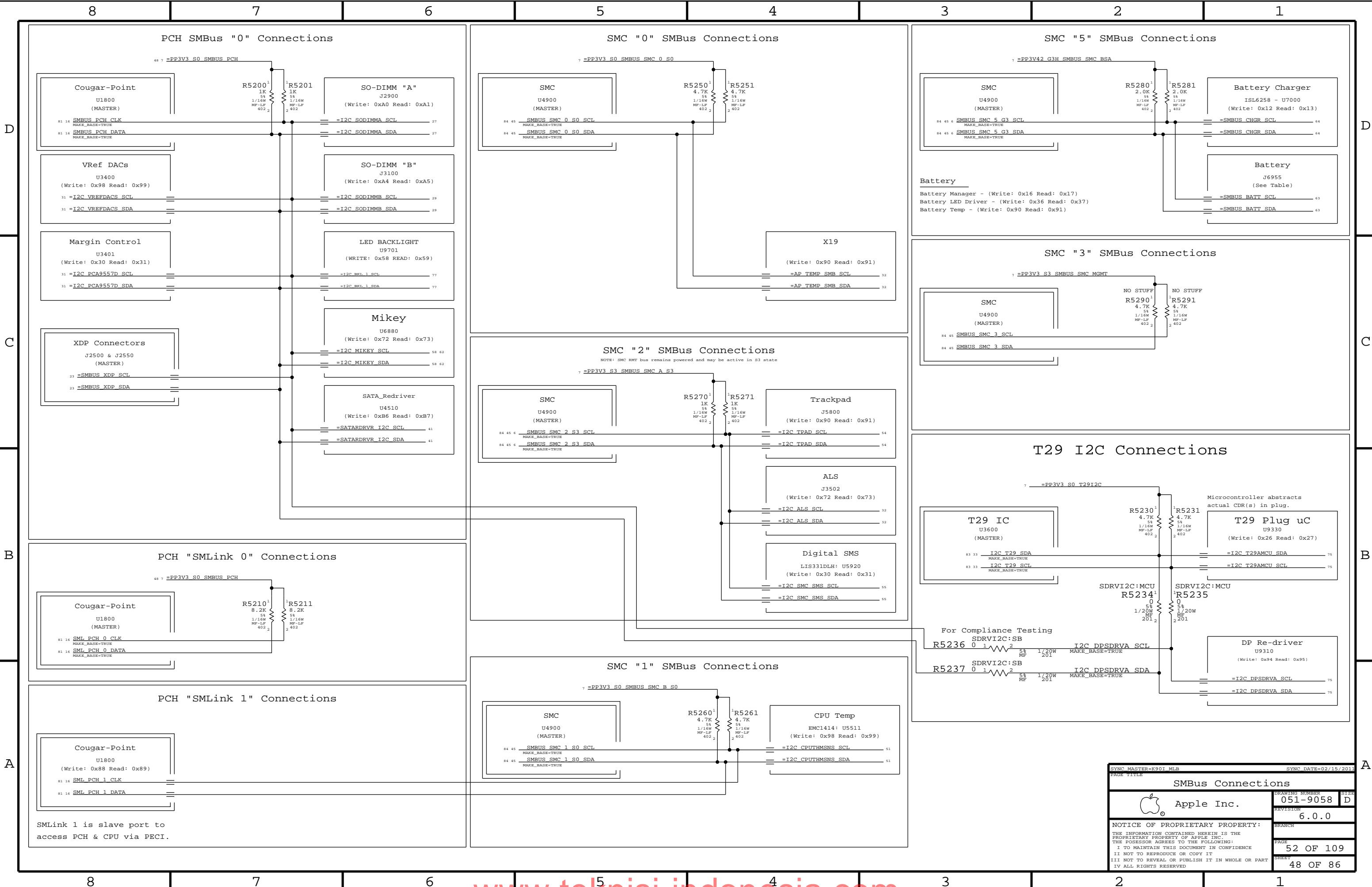


NO STUFF R5022 1/16W 5% PLACE_NEAR=U6100.2:1MM



NO STUFF R5022 1/16W 5% PLACE_NEAR=U6100.2:1MM





8

7

6

5

4

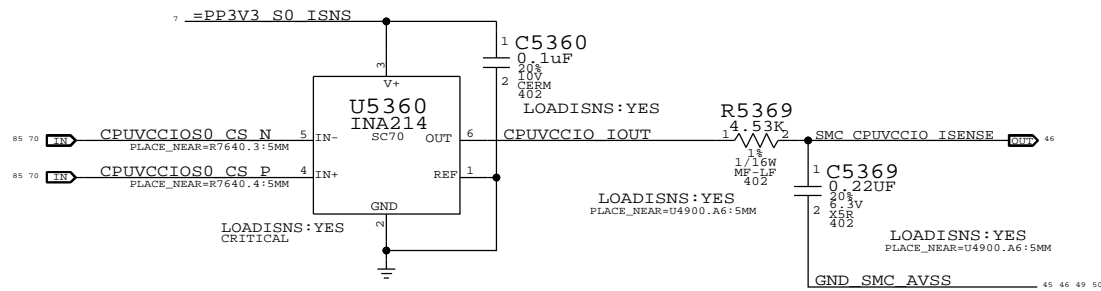
3

2

1

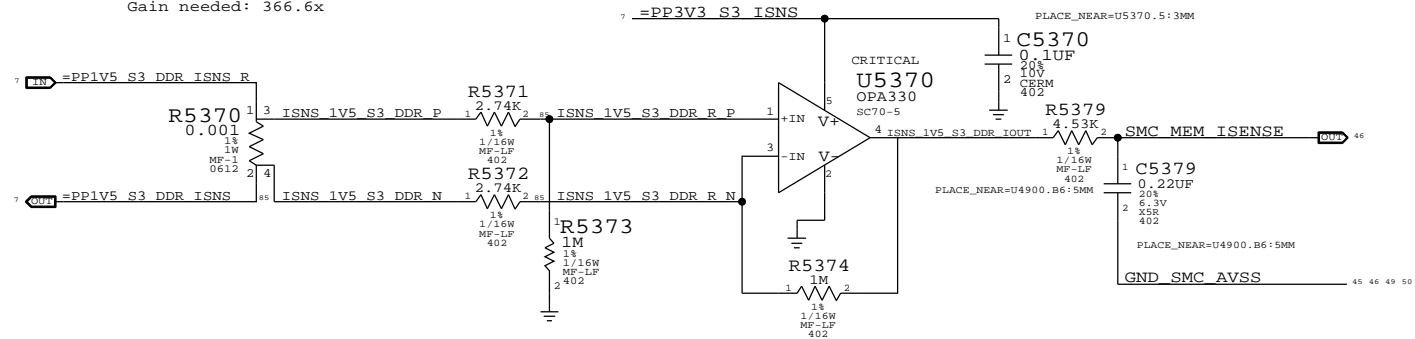
CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 100x, EDP: 20.1 A
Rsense: 0.001 (R7640)
V across Rsense: 20.1 mV
Gain needed: 164.2x



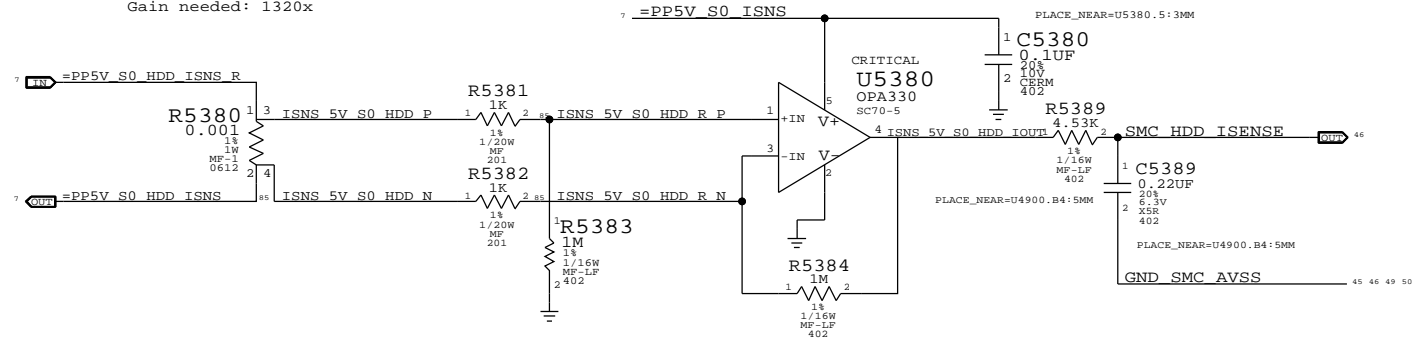
DDR 1.5V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
Gain needed: 366.6x

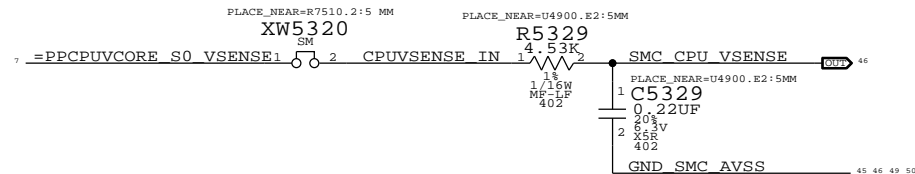


HDD Current Sense (IHDC)

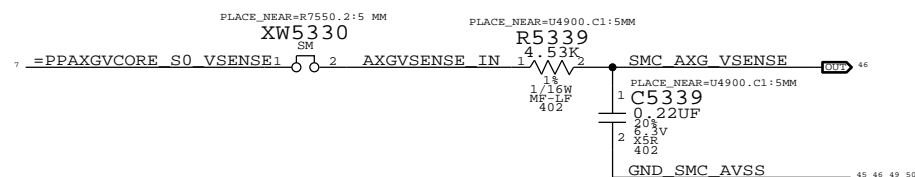
Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R5380)
V across Rsense: 2.5 mV
Gain needed: 1320x



CPU Core Voltage Sense (VC0C)

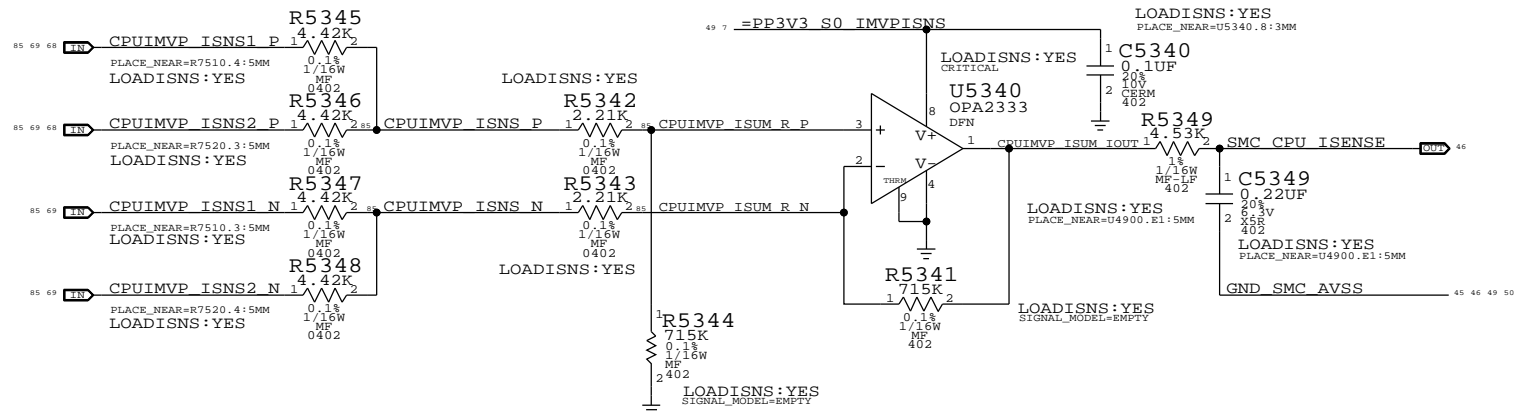


AXG Core Voltage Sense (VN0C)



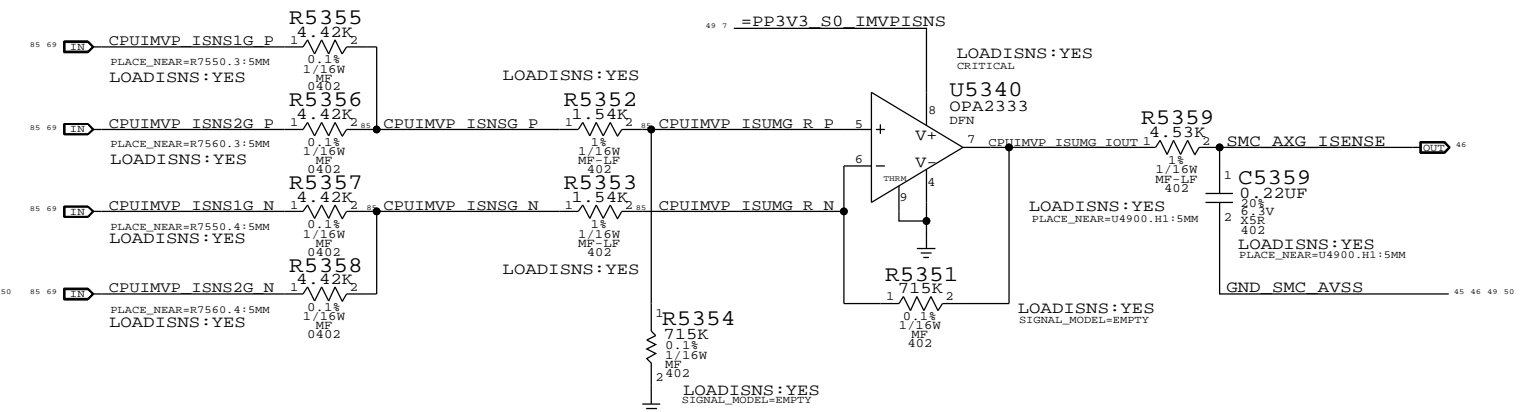
CPU Core Load Side Current Sense (IC0C)

Gain: 161.5x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
Gain needed: 166.1x




AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
Gain needed: 191.3x

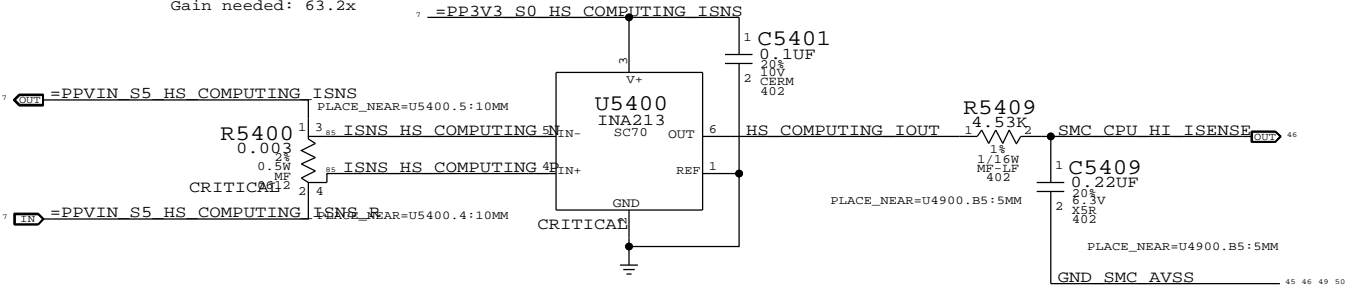


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	3	RES,MTL,FLIM,100K,1/16W,0402,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC MASTER=LINDA J30		SYNC DATE=09/28/2011	
PAGE TITLE			
Power Sensors: Load Side			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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		PAGE	53 OF 109
		SHEET	49 OF 86

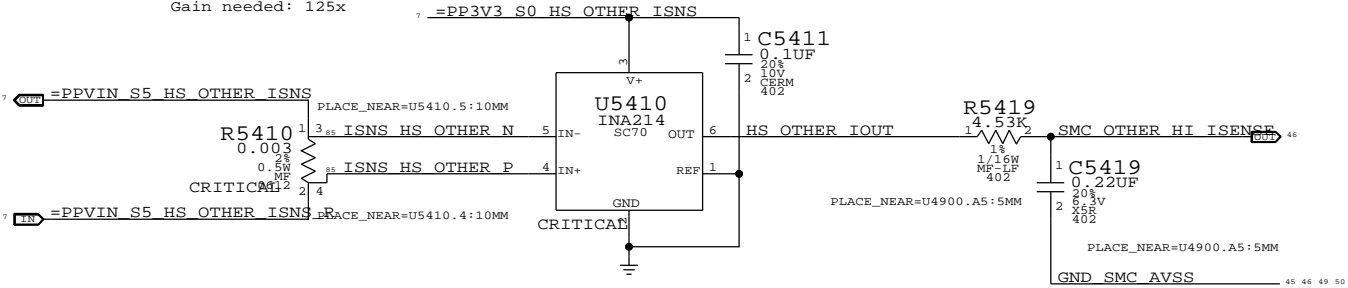
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
Gain needed: 63.2x



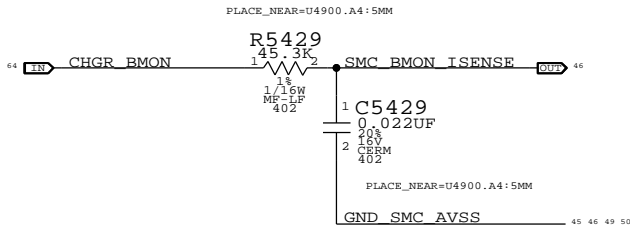
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
Gain needed: 125x



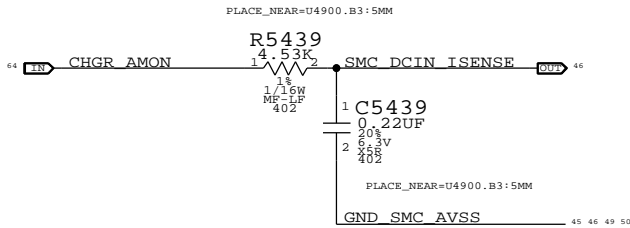
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Current Measured: 9.2 A

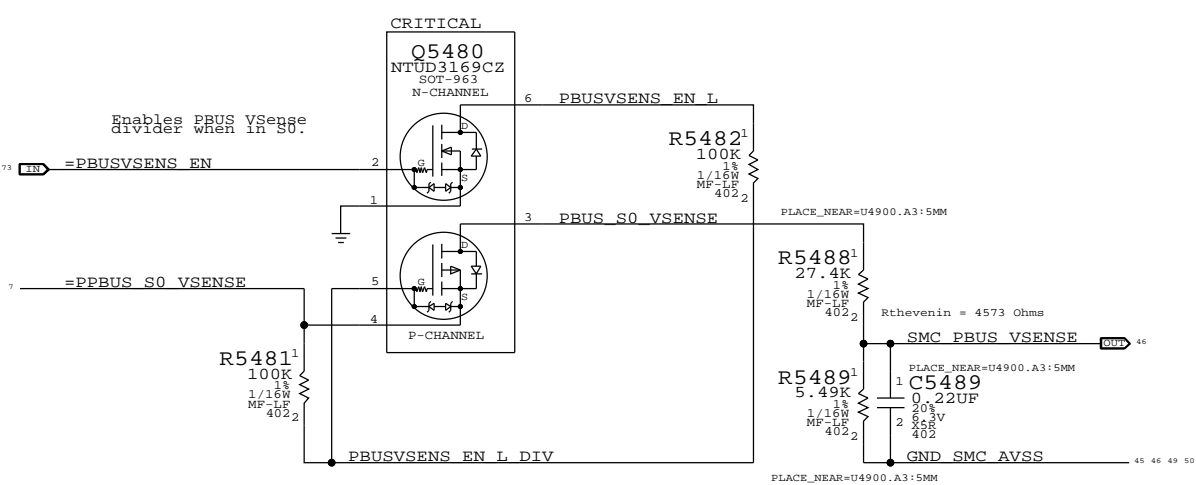


DC-In (AMON) Current Sense (ID0R)

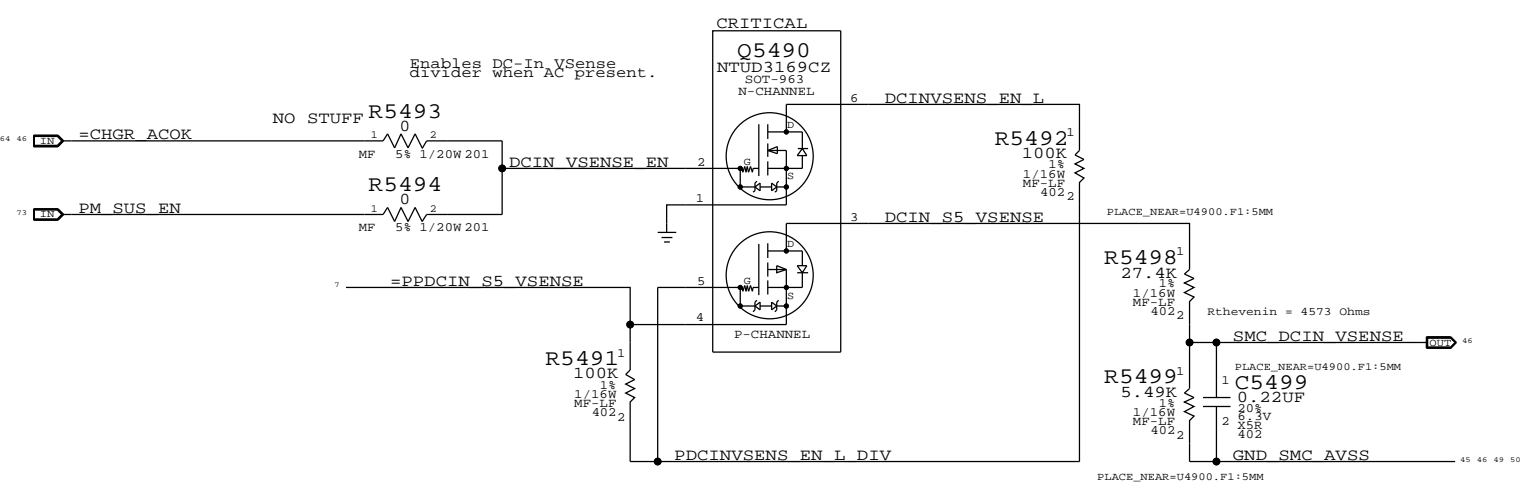
Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Current Measured: 8.3 A




PBUS Voltage Sense & Enable (VP0R)



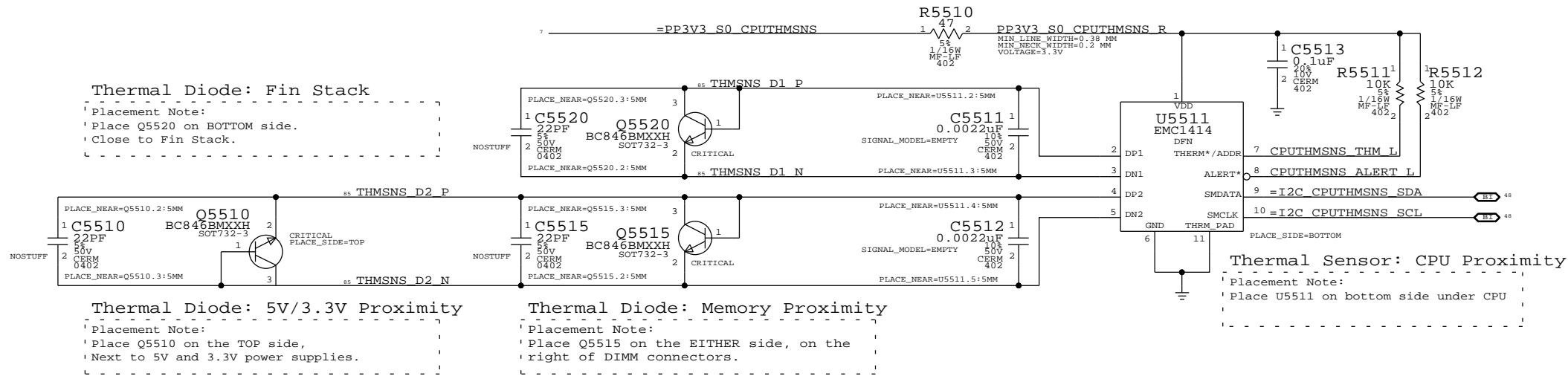
DC In Voltage Sense & Enable (VD0R)



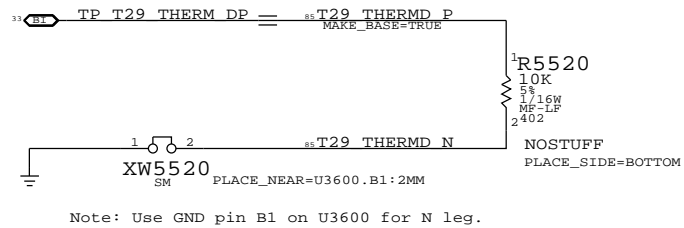
SYNC MASTER=YONAS J30		SYNC DATE=11/03/2011	
PAGE TITLE			
Power Sensors: High Side			
	Apple Inc.	DRAWING NUMBER	051-9058
		SIZE	D
		REVISION	6.0.0
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Thermal Sensor:
CPU Proximity, Fin Stack, Memory Proximity, 5V/3.3V Proximity

I2C Write: 0x98, I2C Read: 0x99



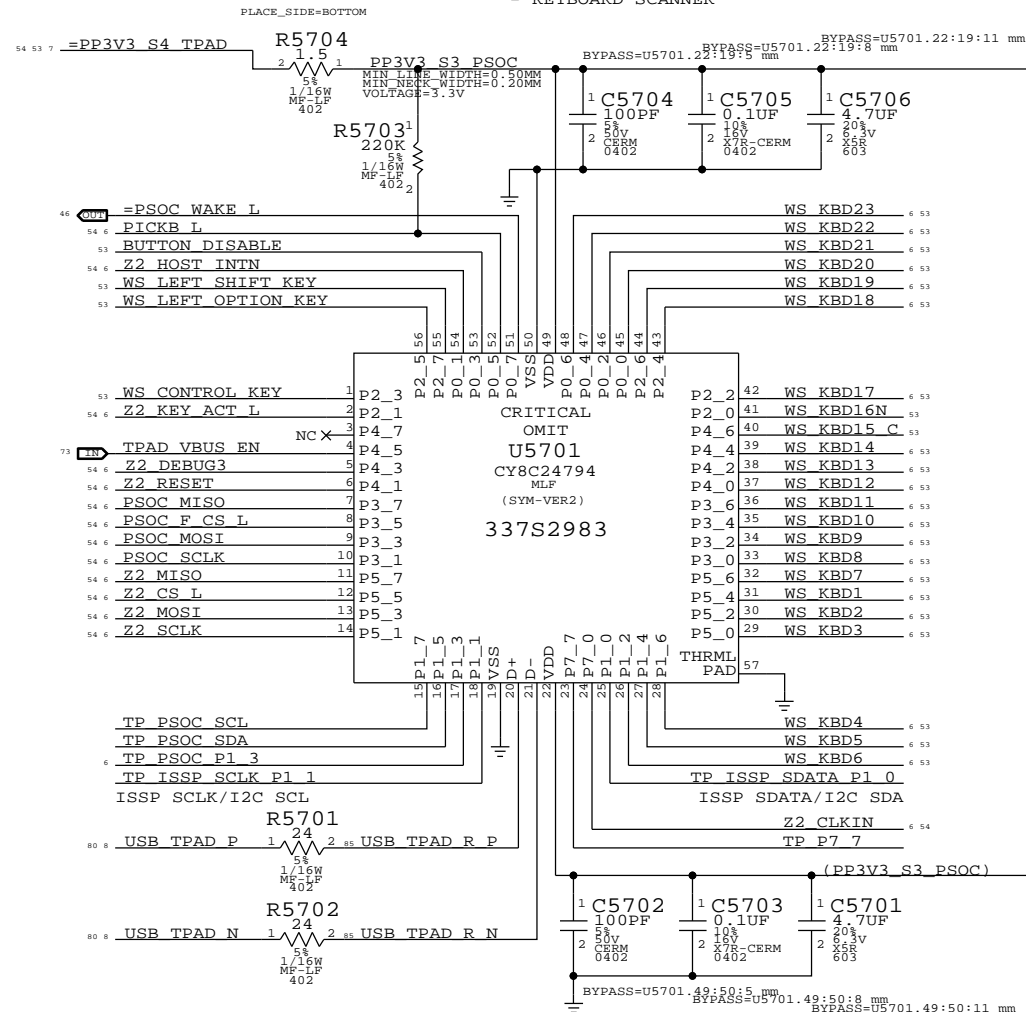
Thermal Sensor: T29 Die



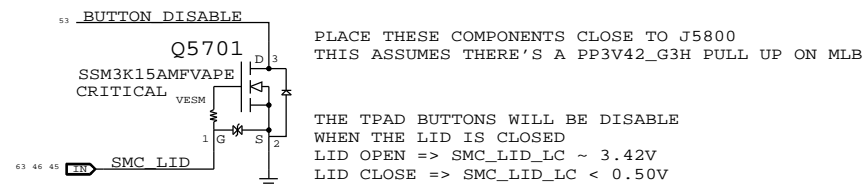
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Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	051-9058
		SIZE	D
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		BRANCH	
		PAGE	55 OF 109
		SHEET	51 OF 86

PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

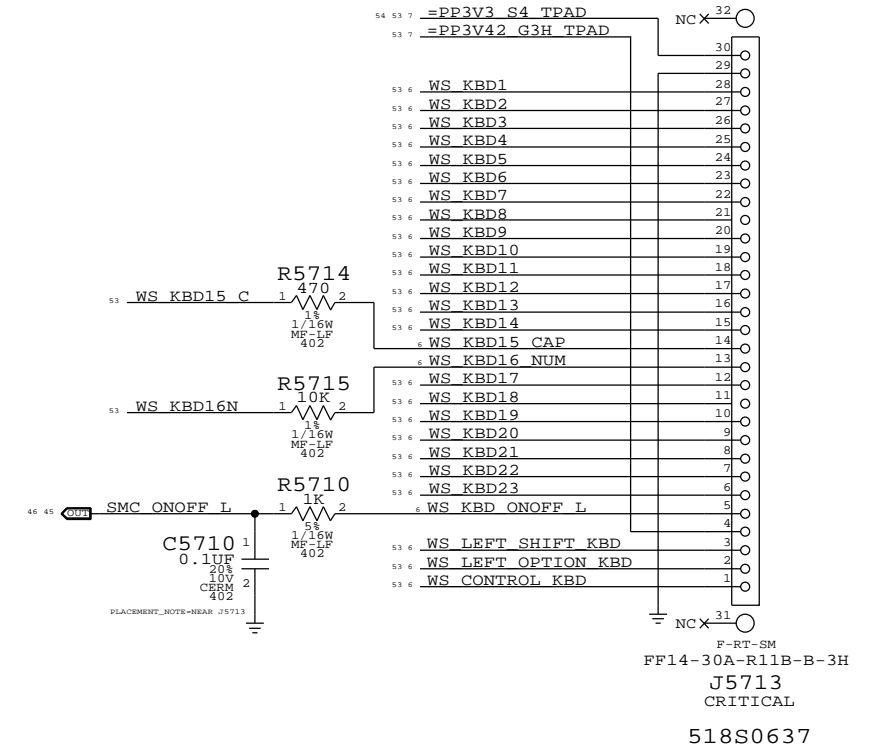


TPAD Buttons Disable



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6
		80UA		0.204 V	16.32E-6
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6
		14MA (MAX)		0.021 V	294E-6
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6

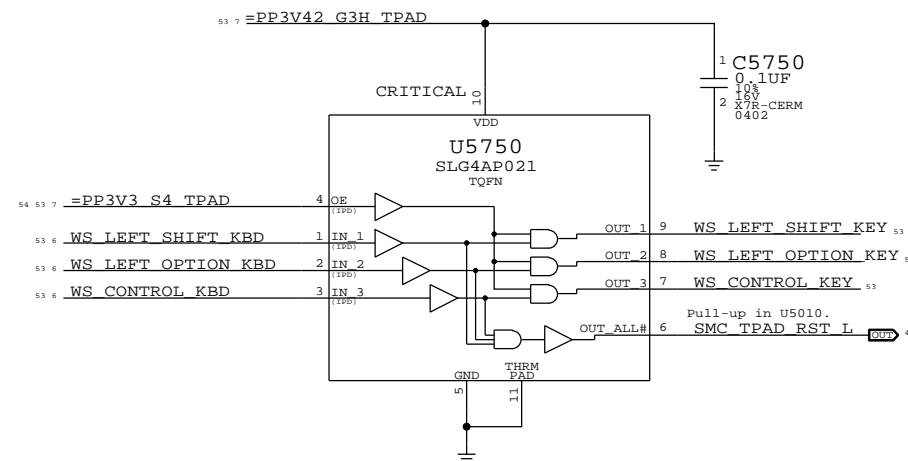
Keyboard Connector




SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

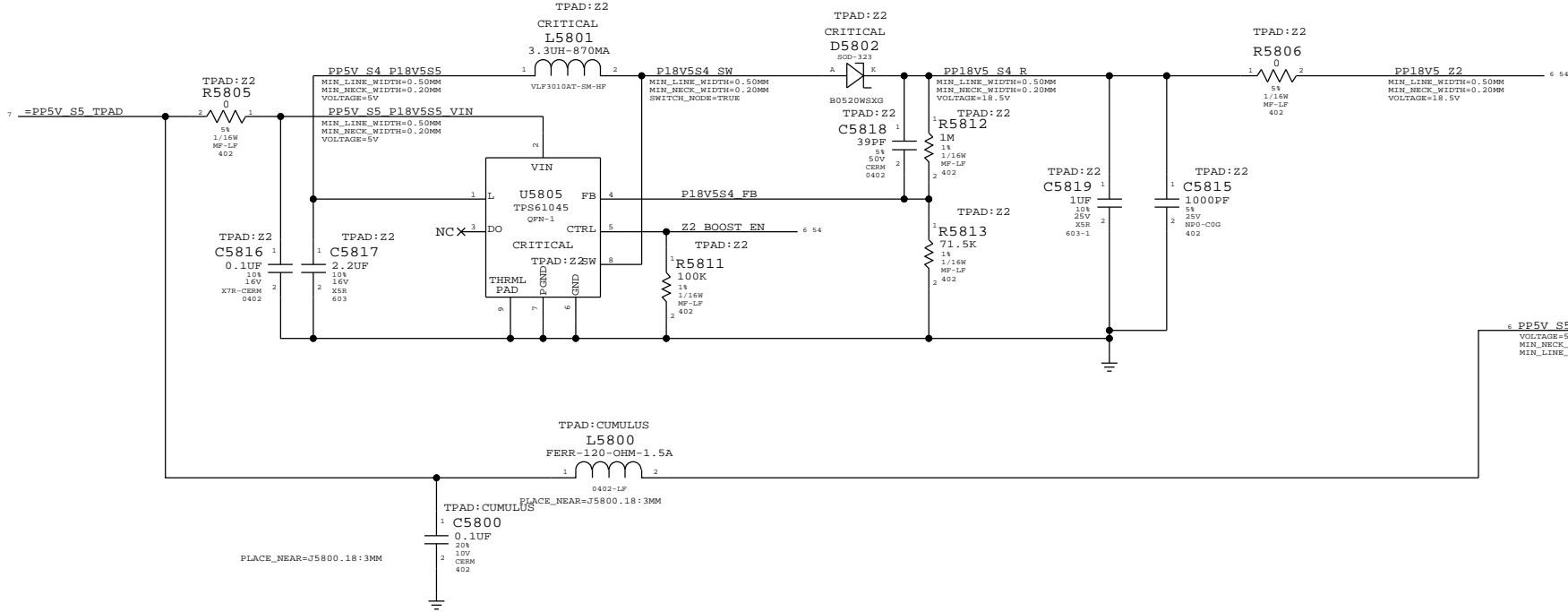
Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).



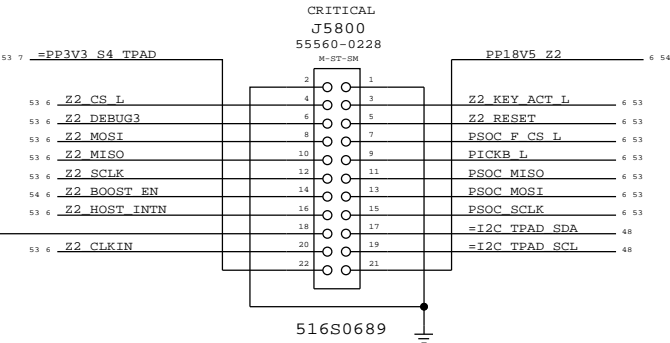
SYNC MASTER=J31 MLB		SYNC DATE=07/01/2011	
PAGE TITLE			
WELLSPRING 1			
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			051-9058
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		REVISION	
		6.0.0	
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BOOSTER +18.5VDC FOR SENSORS

- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED

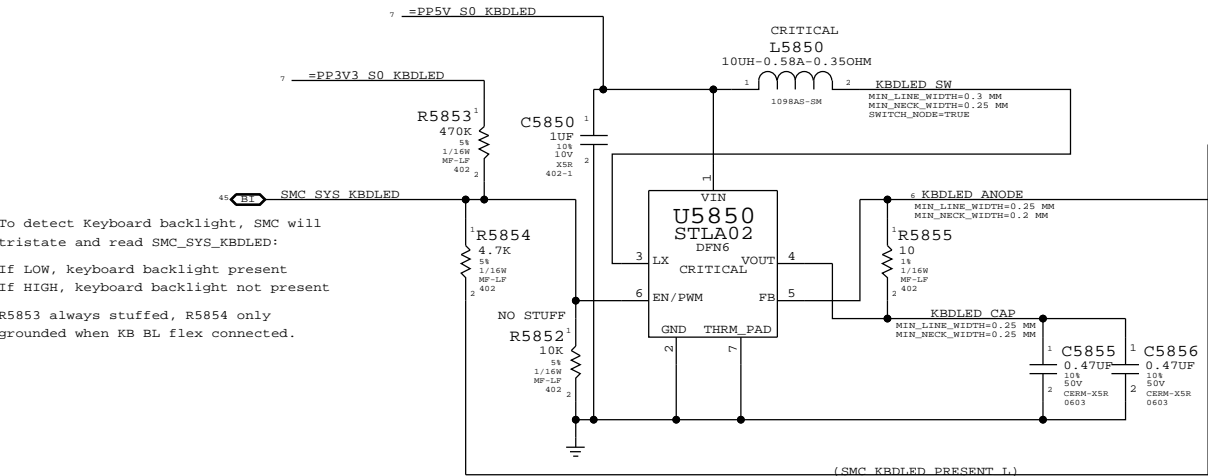


IPD Flex Connector

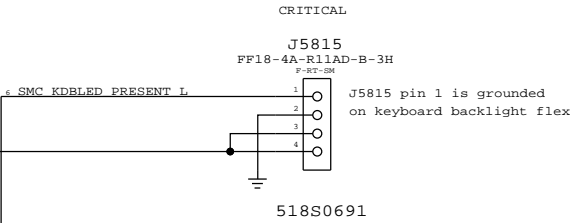


PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX

Keyboard Backlight Driver & Detection

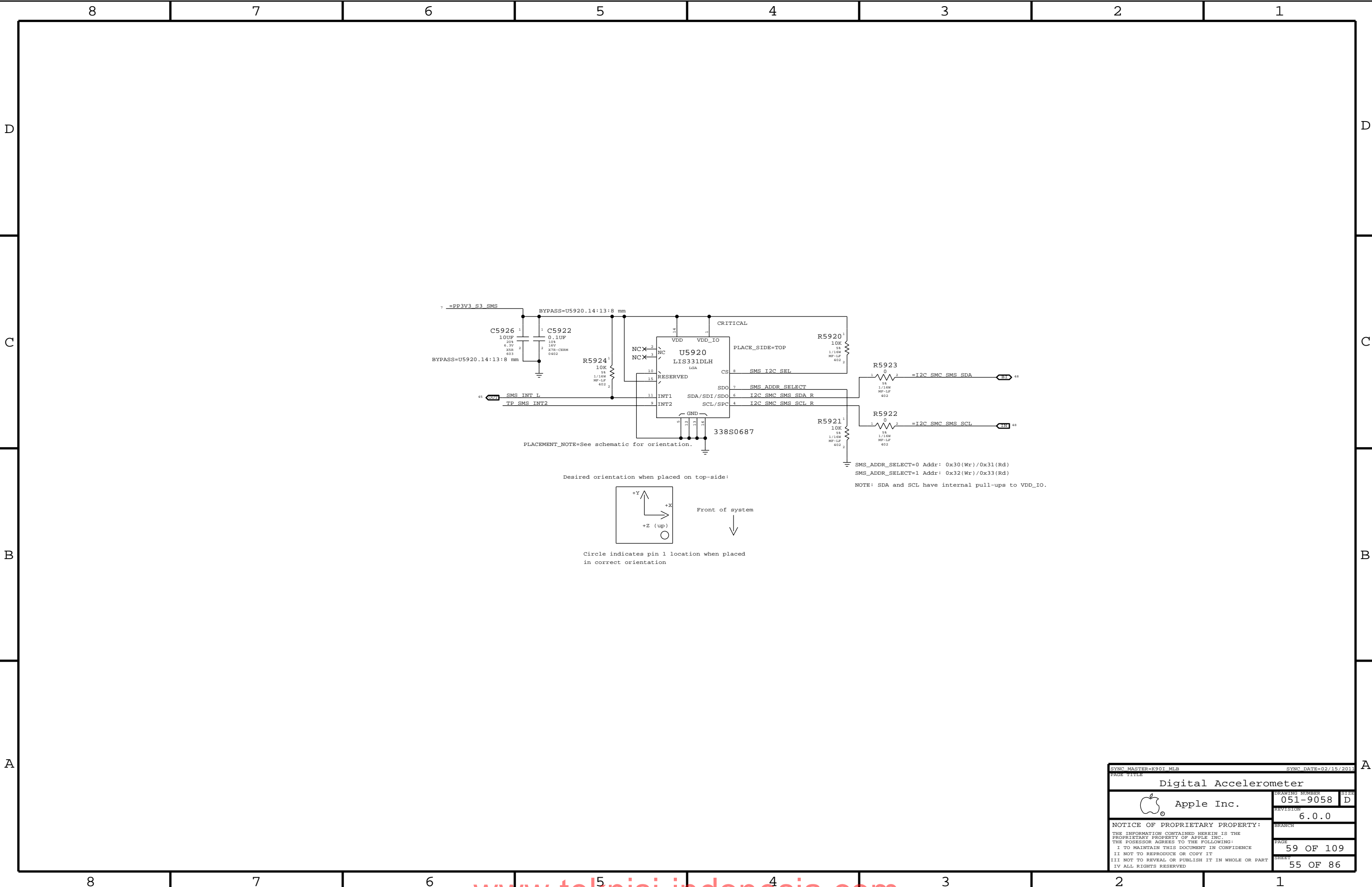



Keyboard Backlight Connector

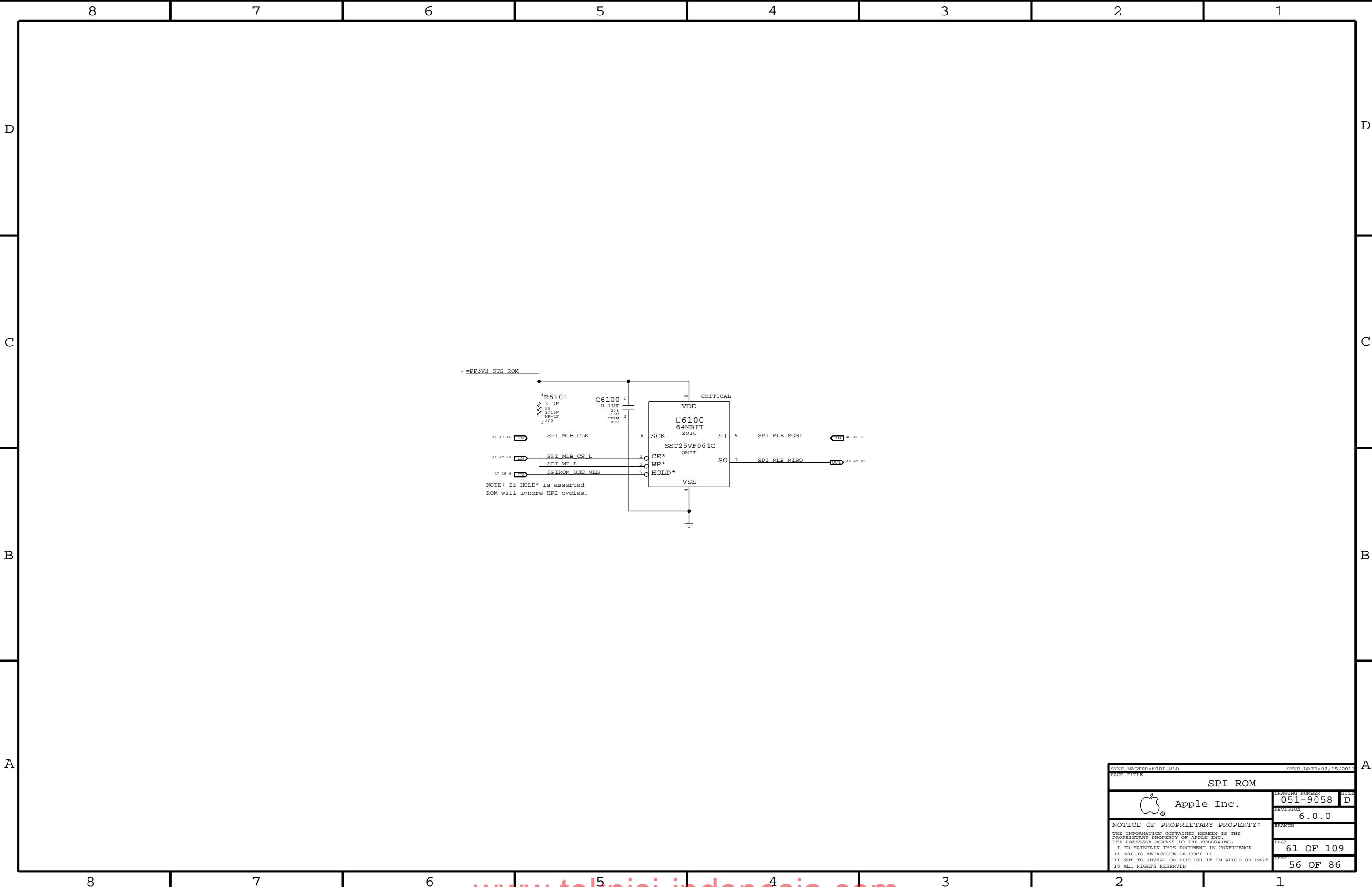


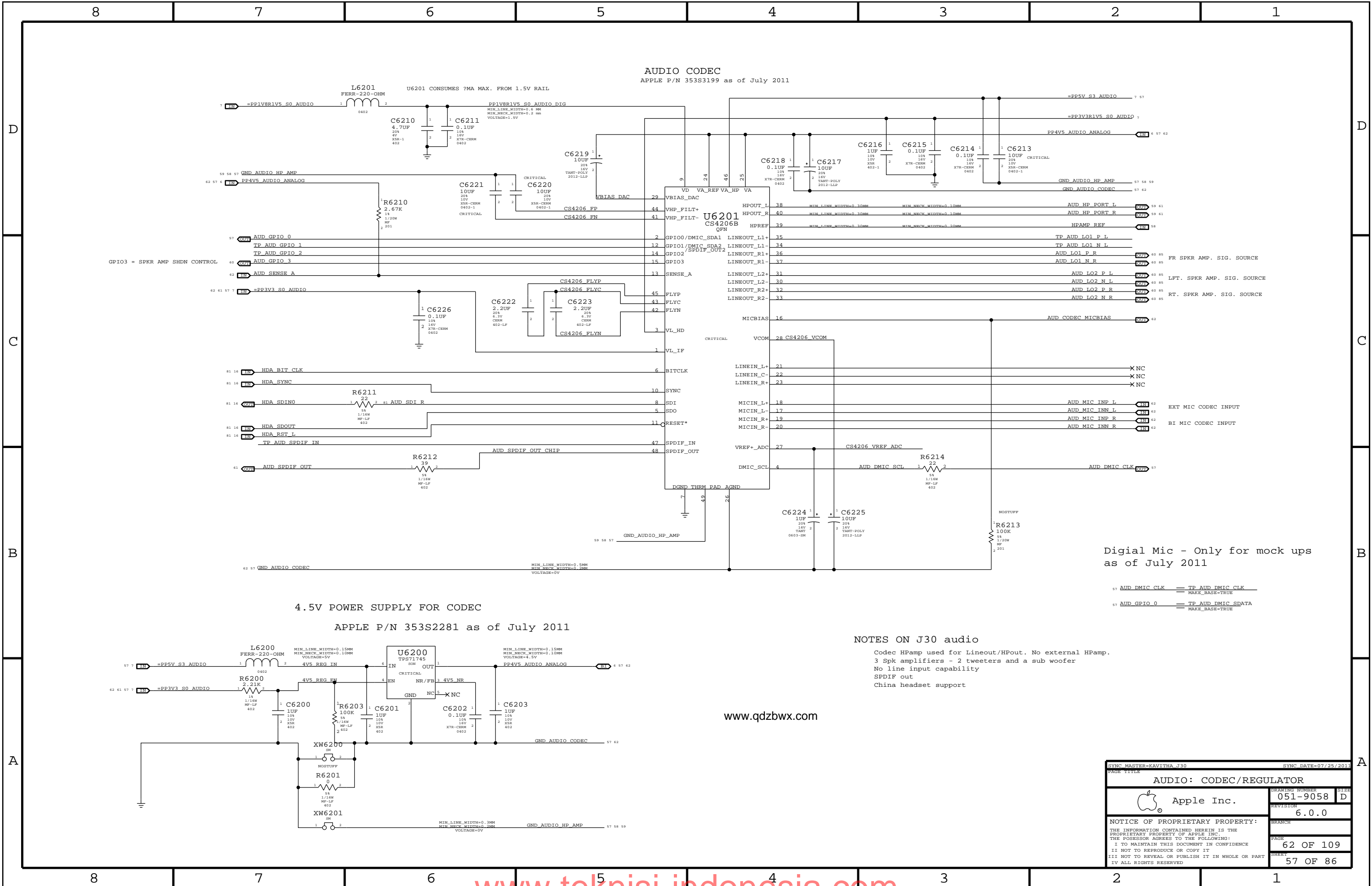
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
If LOW, keyboard backlight present
If HIGH, keyboard backlight not present
R5853 always stuffed, R5854 only grounded when KB BL flex connected.

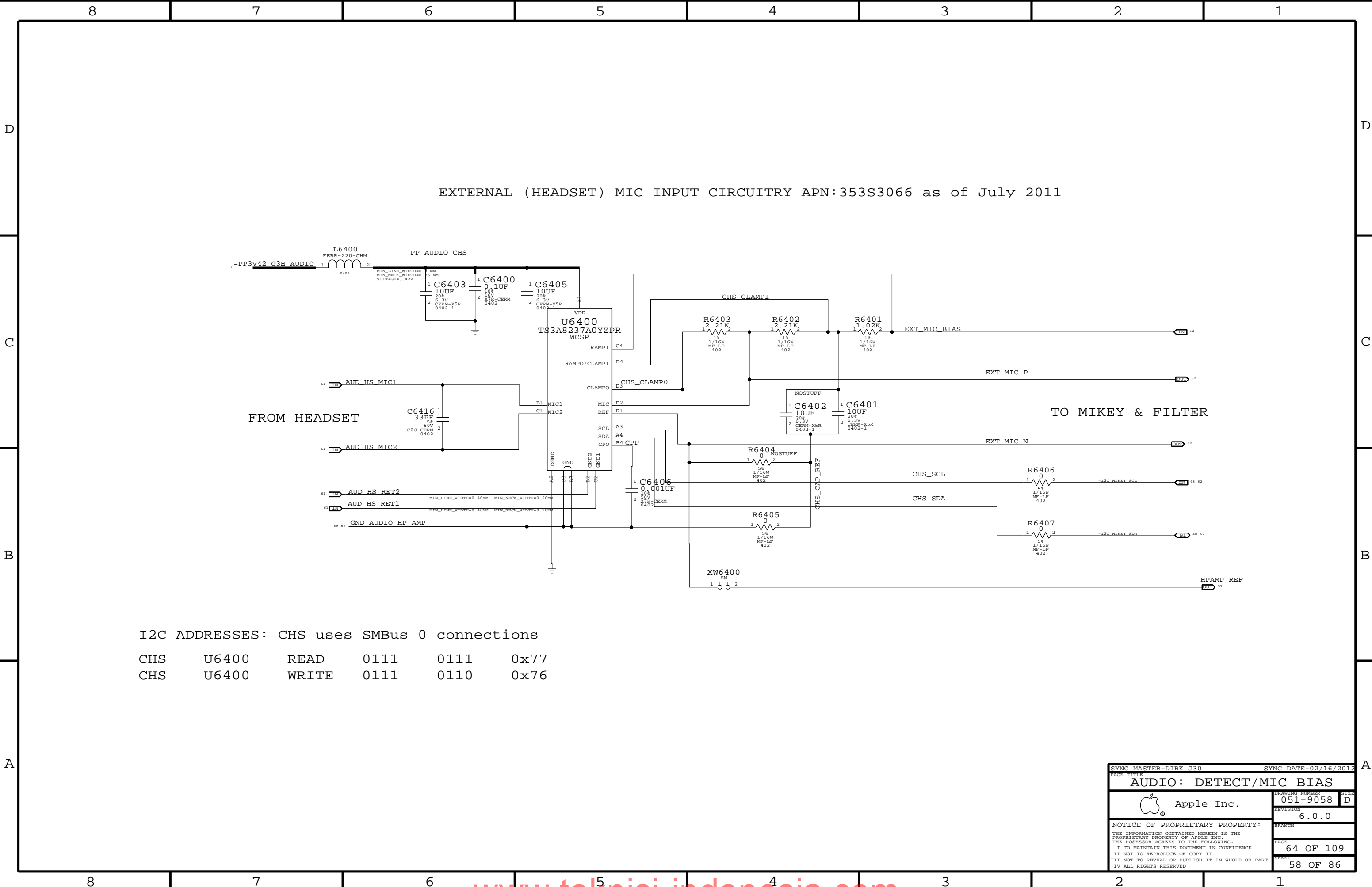
WELLSPRING 2		051-9058	
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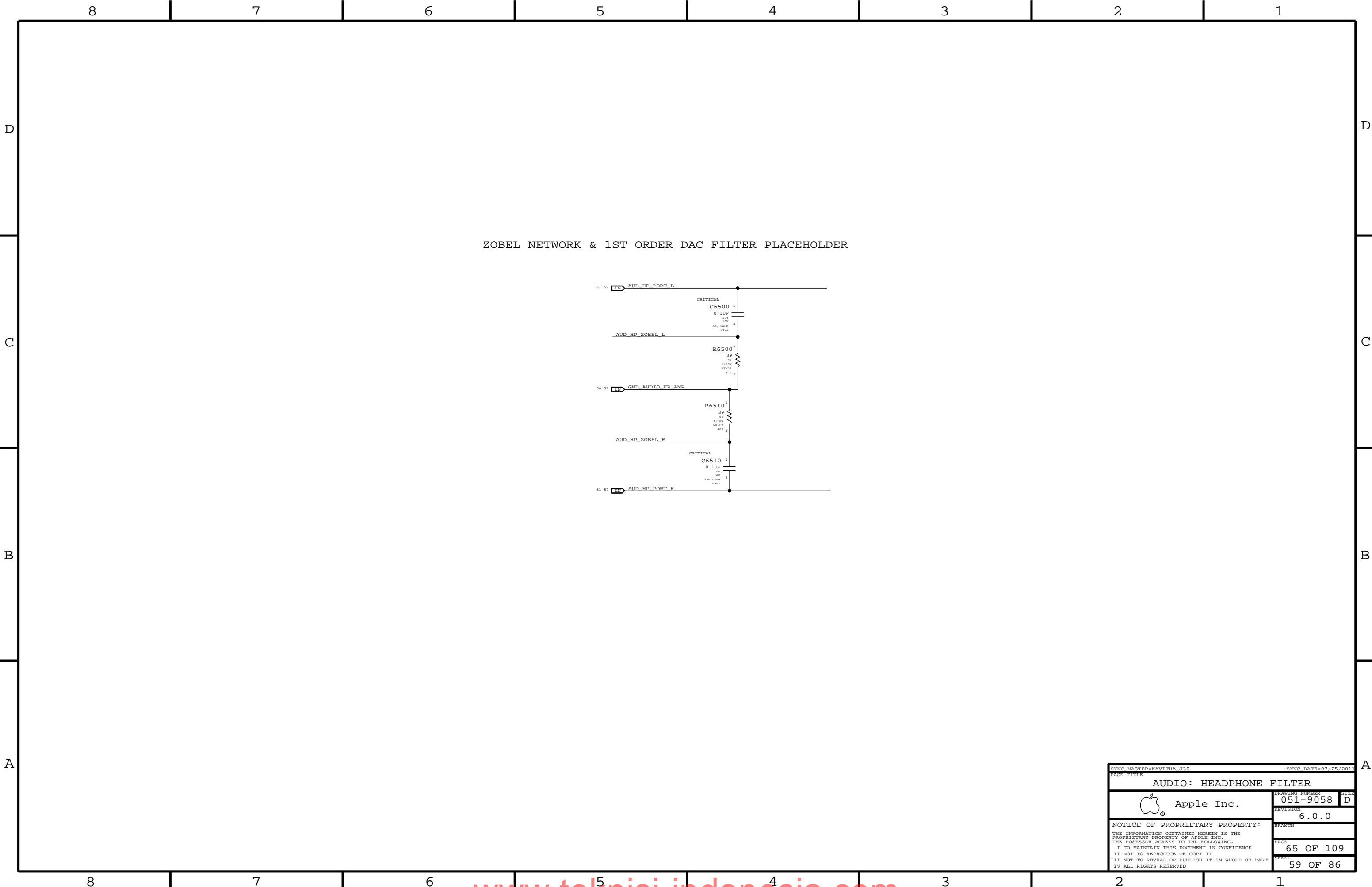



SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
Digital Accelerometer			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		6.0.0
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SYNC MASTER=KAVITHA J30		SYNC DATE=07/25/2013	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9058		D
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	6.0.0		
		PAGE	
		65 OF 109	
		SHEET	
		59 OF 86	

D

C

B

A

D

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A

SATELLITE & SUB TWEETER AMPLIFIER

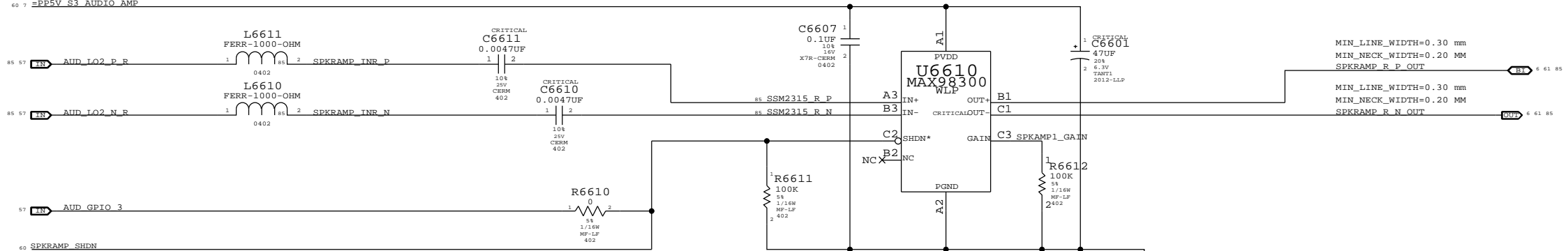
APN:353S2888 as of July 2011

SATELLITE	FC=1.2kHz typical
SUB	FC= 172 HZ typical
GAIN	3DB with Rin=28k typical

Gain Pin	Gain dB
Connect to VDD	12
Connect to VDD through 100k	9
Not connected	6
Connect to GND through 100k	3
Connect to GND	0

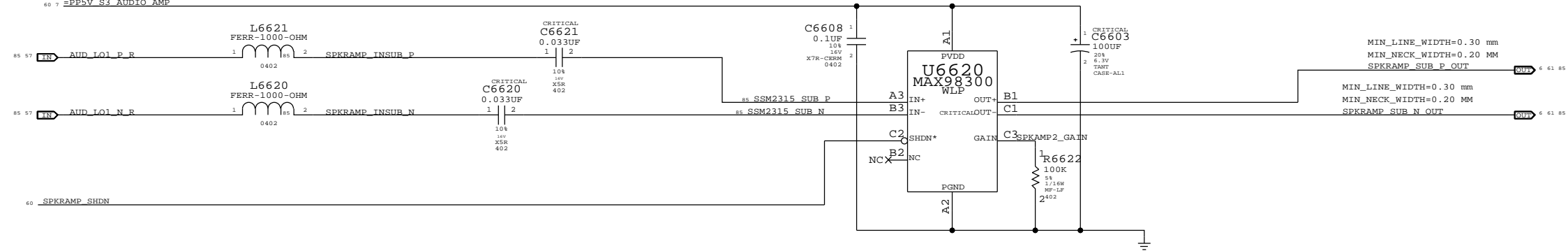
ALIAS OF PP5VLT_S3, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

60 7 =PP5V_S3 AUDIO AMP



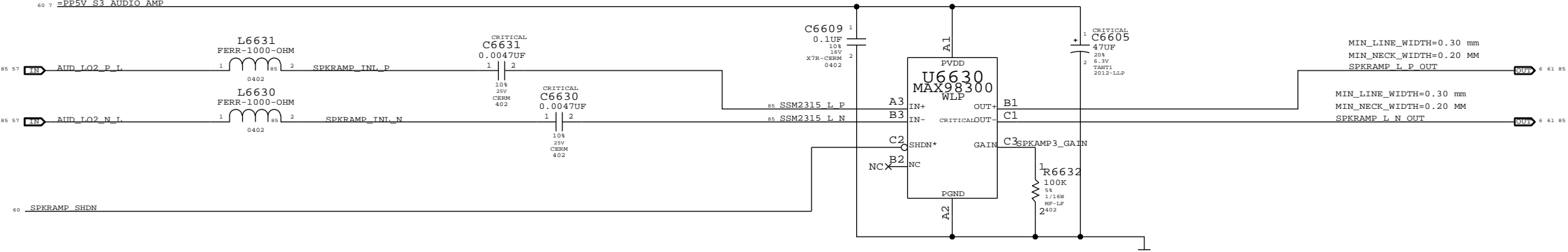
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60 7 =PP5V_S3 AUDIO AMP

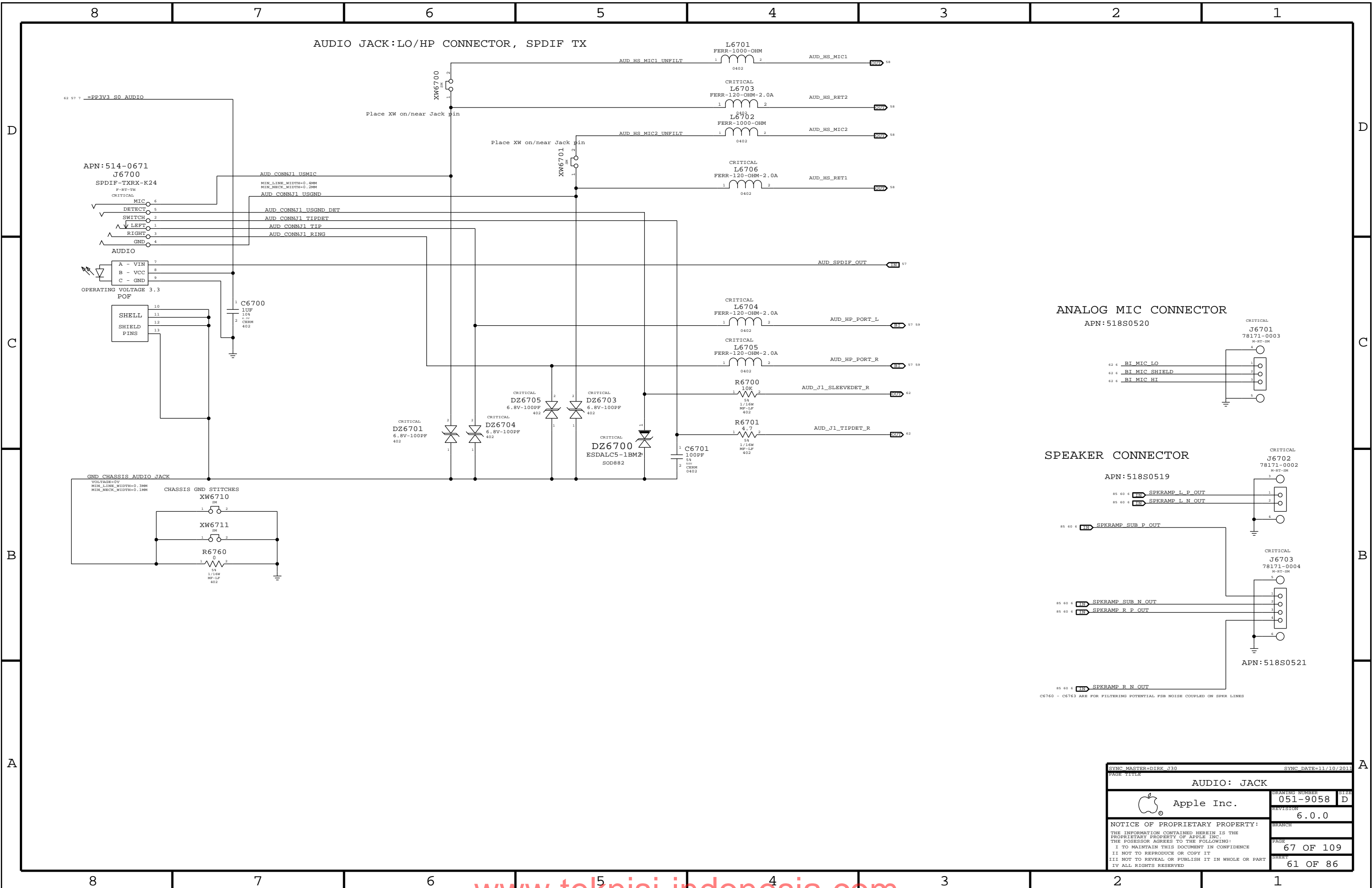



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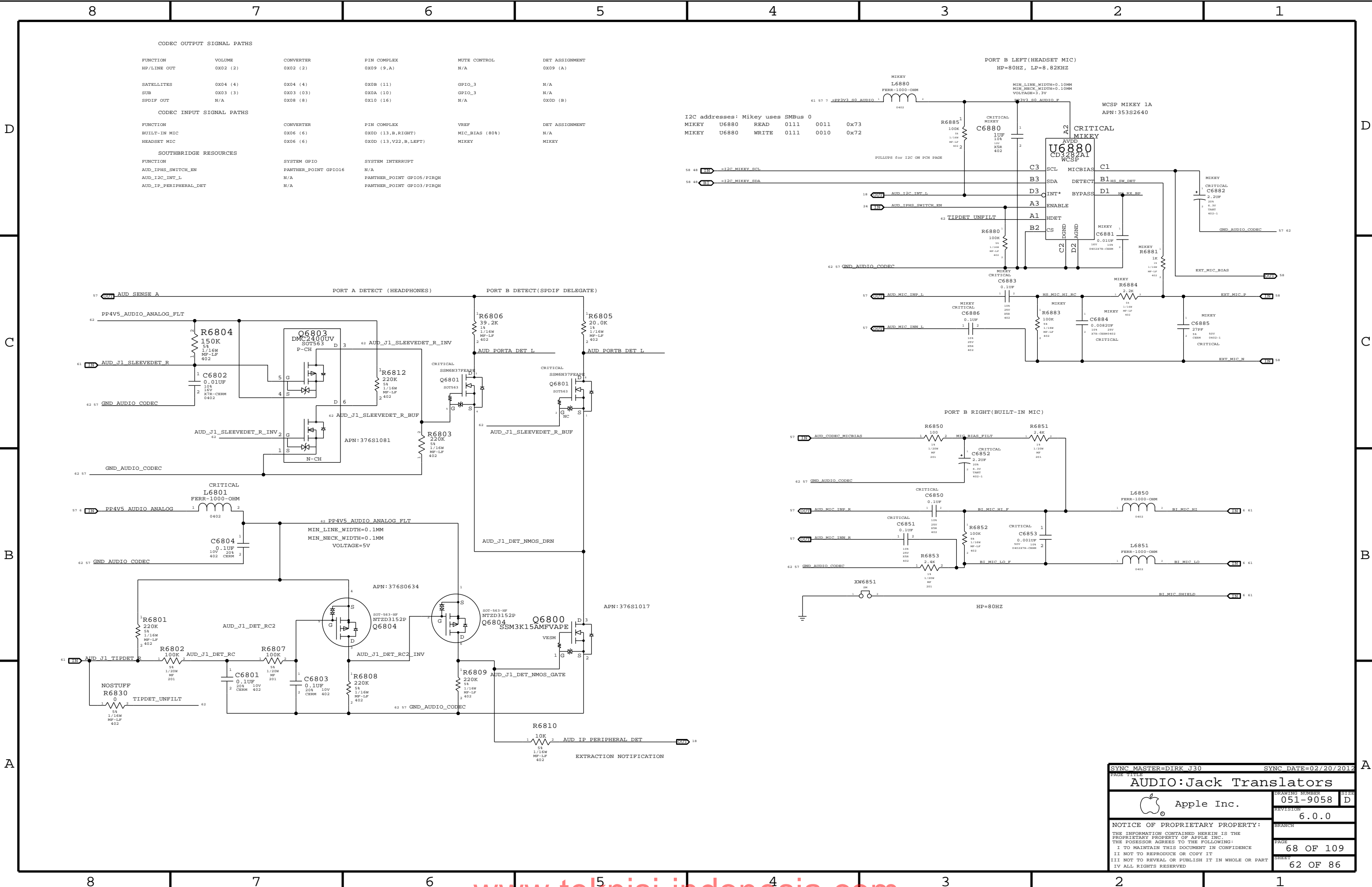
60 7 =PP5V_S3 AUDIO AMP



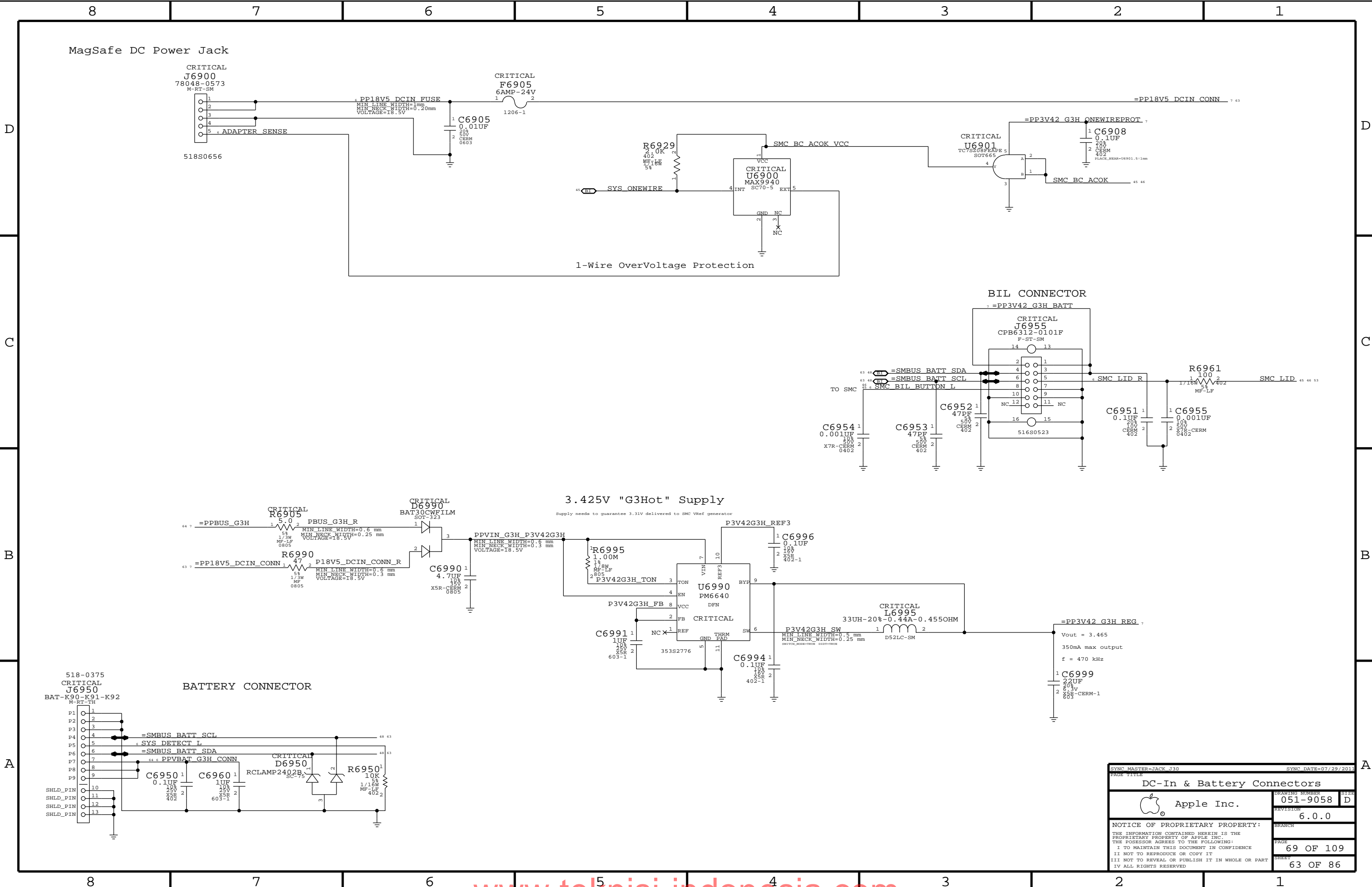
SYNC MASTER=KAVITHA J30		SYNC DATE=07/25/2011	
PAGE TITLE			
AUDIO0: SPEAKER AMP			
 Apple Inc.	DRAWING NUMBER	051-9058	SIZE
	REVISION	6.0.0	D
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


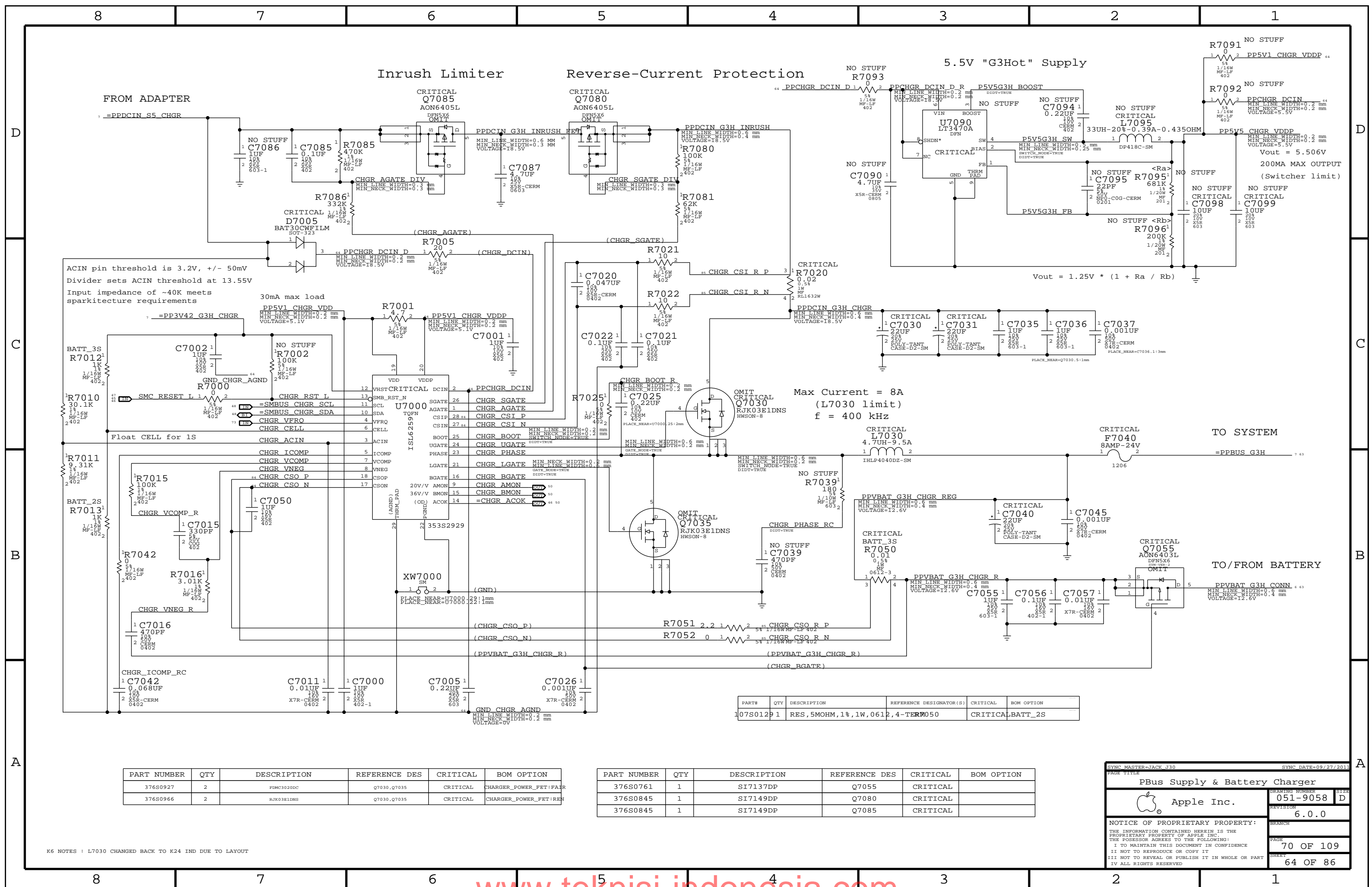
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PAGE TITLE			
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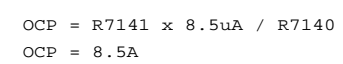
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AUDIO:Jack Translators		051-9058	
Apple Inc.		6.0.0	
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SYNC MASTER=JACK J30		SYNC DATE=07/29/2011	
PAGE TITLE			
DC-In & Battery Connectors			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1C, 1SL9	5870A, PWM, 2BIT-VID, RMOT-S	NSE, 20E7100	CRITICAL	


SYNC MASTER=JACK J30		SYNC DATE=09/28/2011	
PAGE TITLE			
System Agent Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-9058	D
		REVISION	
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PAGE		71 OF 109	
SHEET		65 OF 86	

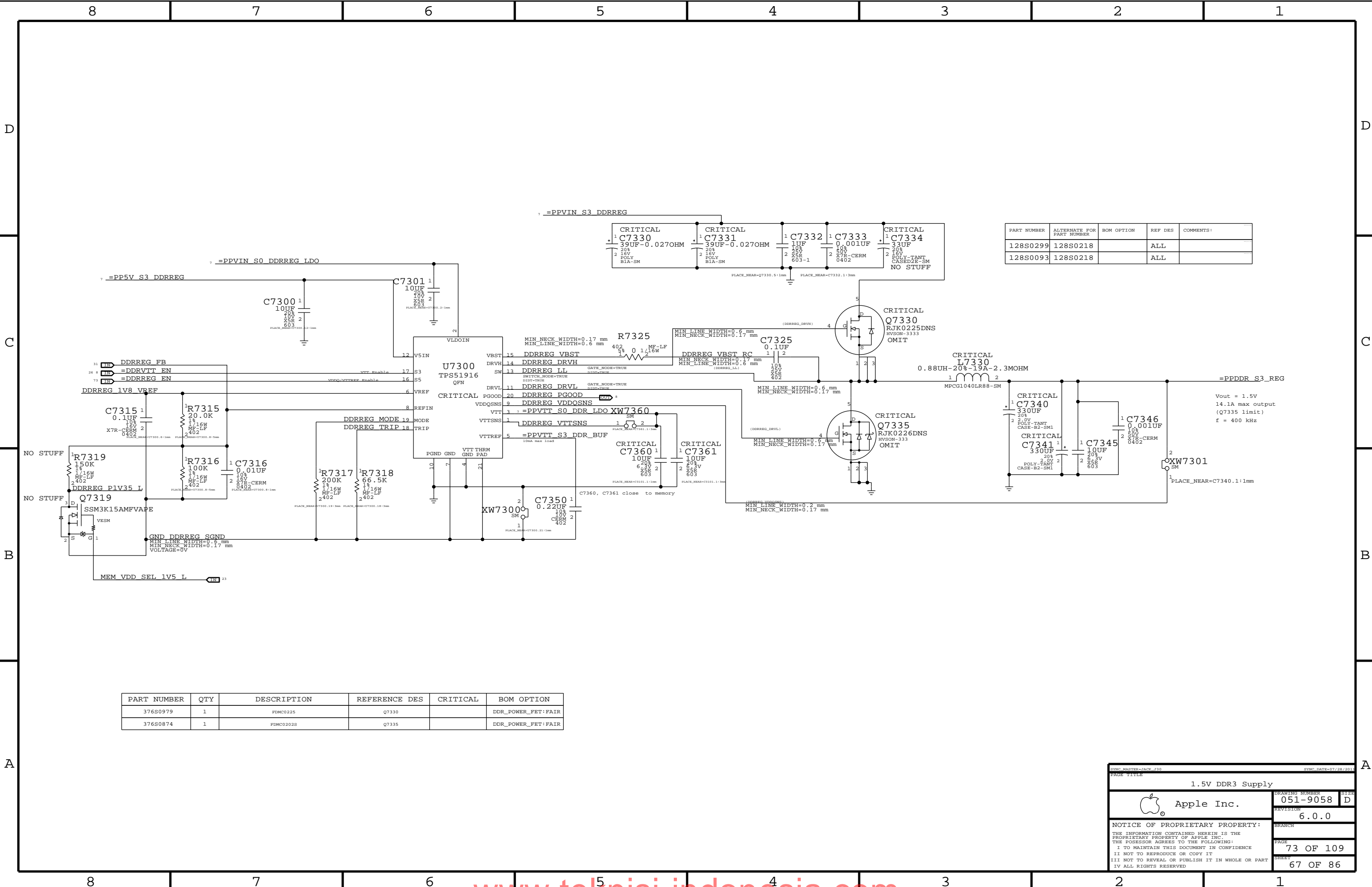
5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0927	1	FDMC3020DC	Q7260		5V_S3_POWER_FET:FAI
376S0928	1	FDMC2514SDC	Q7261		5V_S3_POWER_FET:FAI
376S0960	1	RJK03E1DMS	Q7260		5V_S3_POWER_FET:REN
376S0895	1	RJK03E0DMS	Q7261		5V_S3_POWER_FET:REN

SYNC MASTER=JACK J30		SYNC DATE=08/22/2011	
PAGE TITLE			
5V/3.3V SUPPLY			
	Apple Inc.	DRAWING NUMBER	051-9058
		SIZE	D
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		PAGE	72 OF 109
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0979	1	FDMC0225	Q7330		DDR_POWER_FET:FAIR
376S0874	1	FDMC0202S	Q7335		DDR_POWER_FET:FAIR

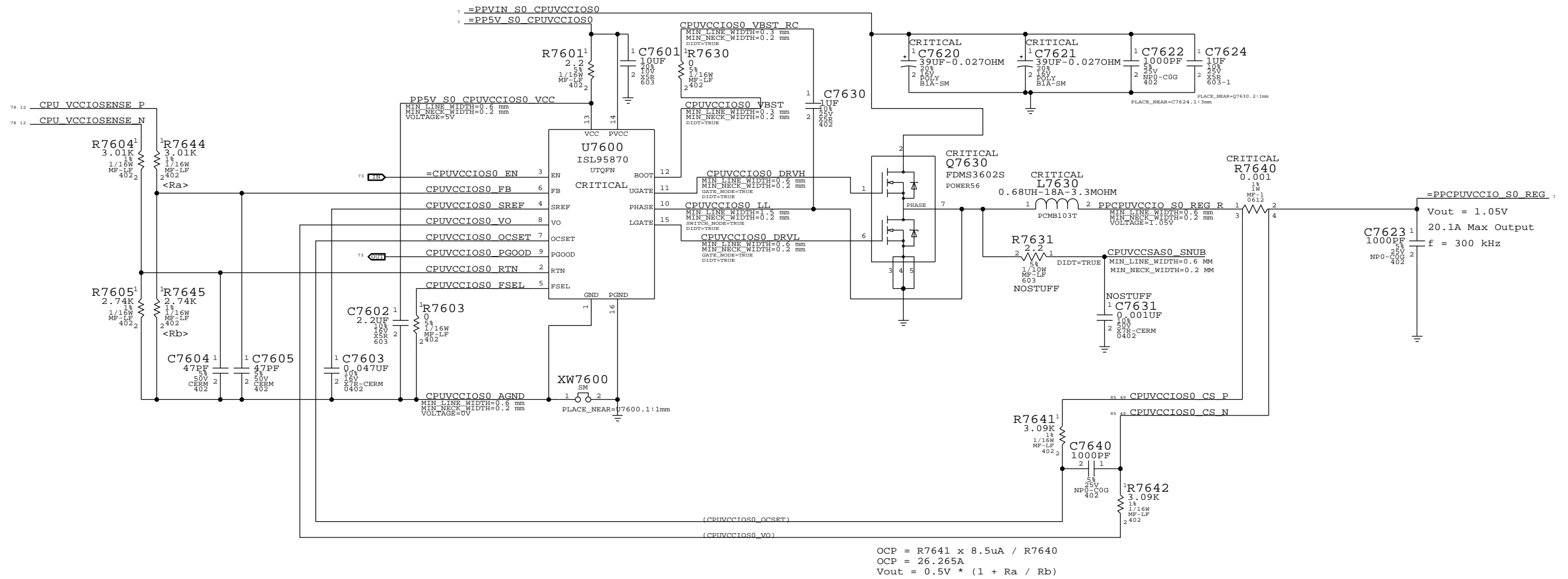
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	


1.5V DDR3 Supply			
Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
		BRANCH	
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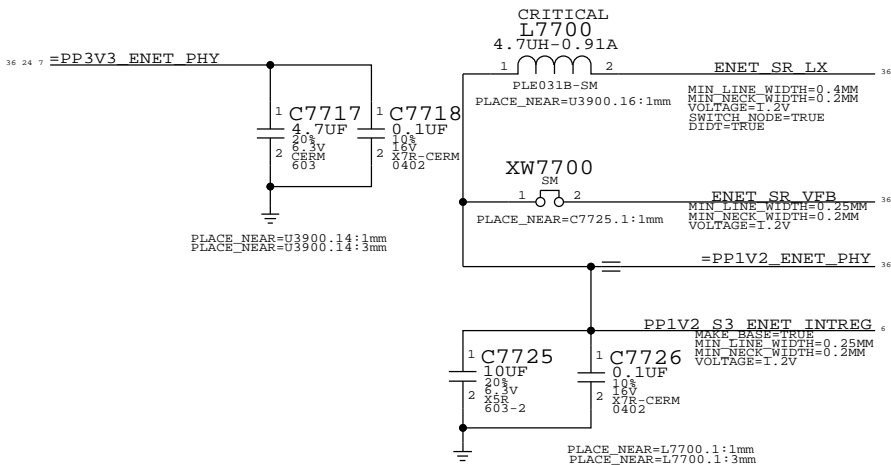


CPU VCCIO (1.05V S0) Regulator



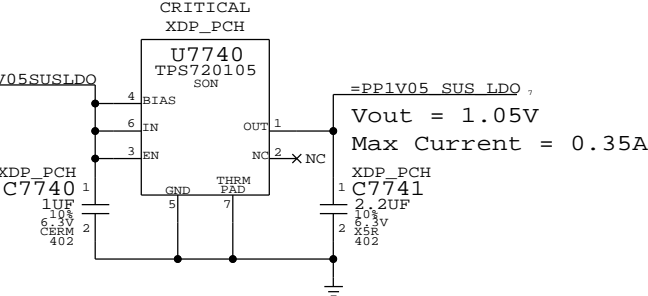
SYNC MASTER=JACK J30		SYNC DATE=09/28/2011	
PAGE TITLE			
CPUVCCIO (1.05V) Power Supply			
	DRAWING NUMBER		SIZE
	051-9058		D
	REVISION		
Apple Inc.		6.0.0	
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CAESAR IV 1.2V INT.VR CMPTS



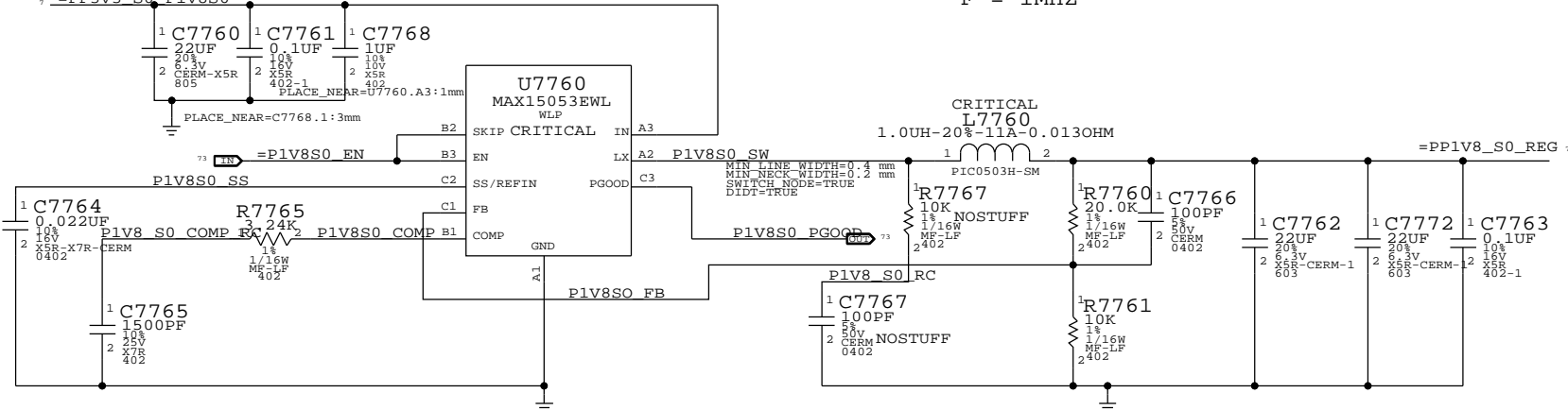
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



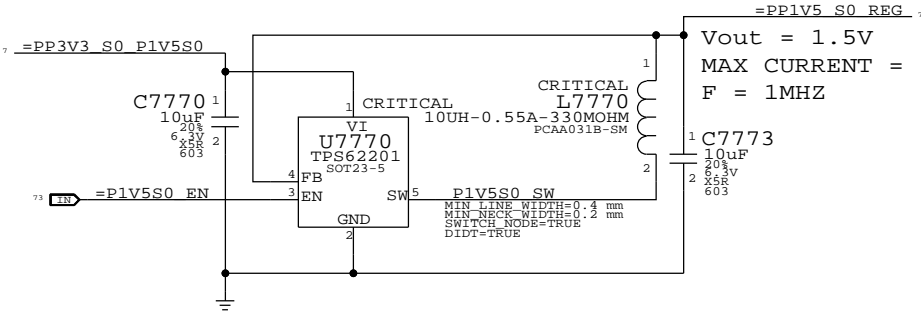
1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



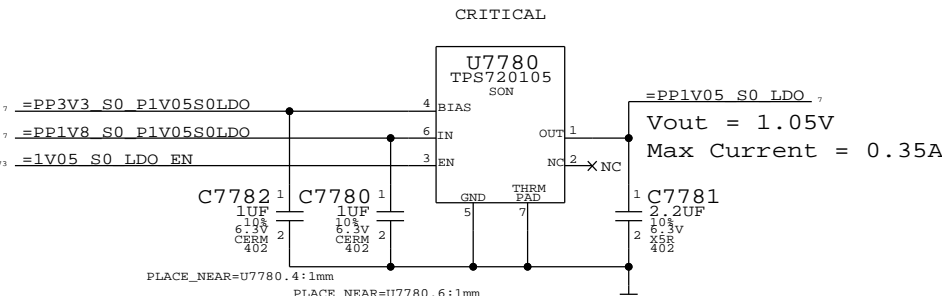
1.5V S0 Switcher


Vout = 1.5V
MAX CURRENT = 0.3A
F = 1MHZ

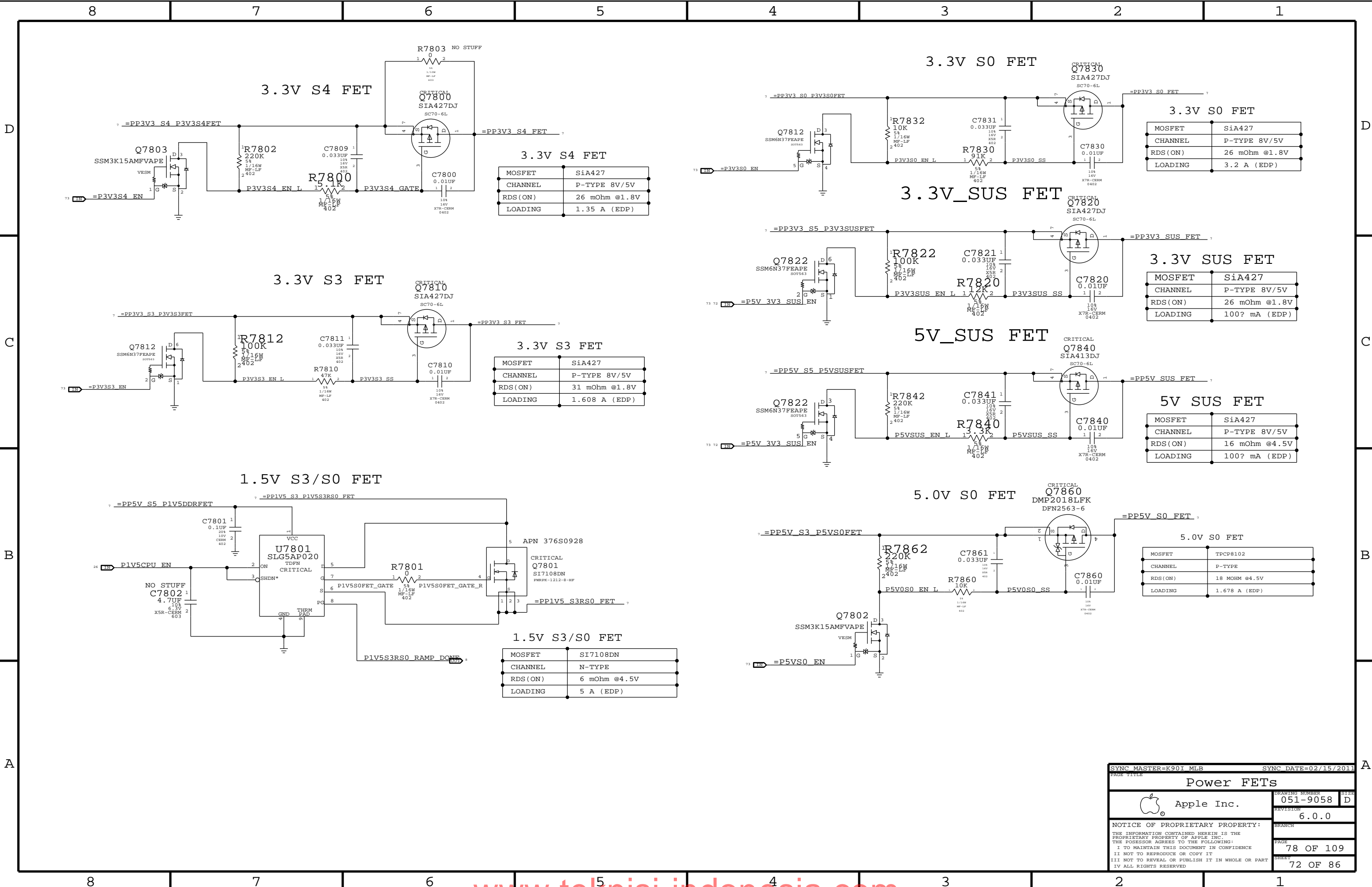


1.05V S0 LDO

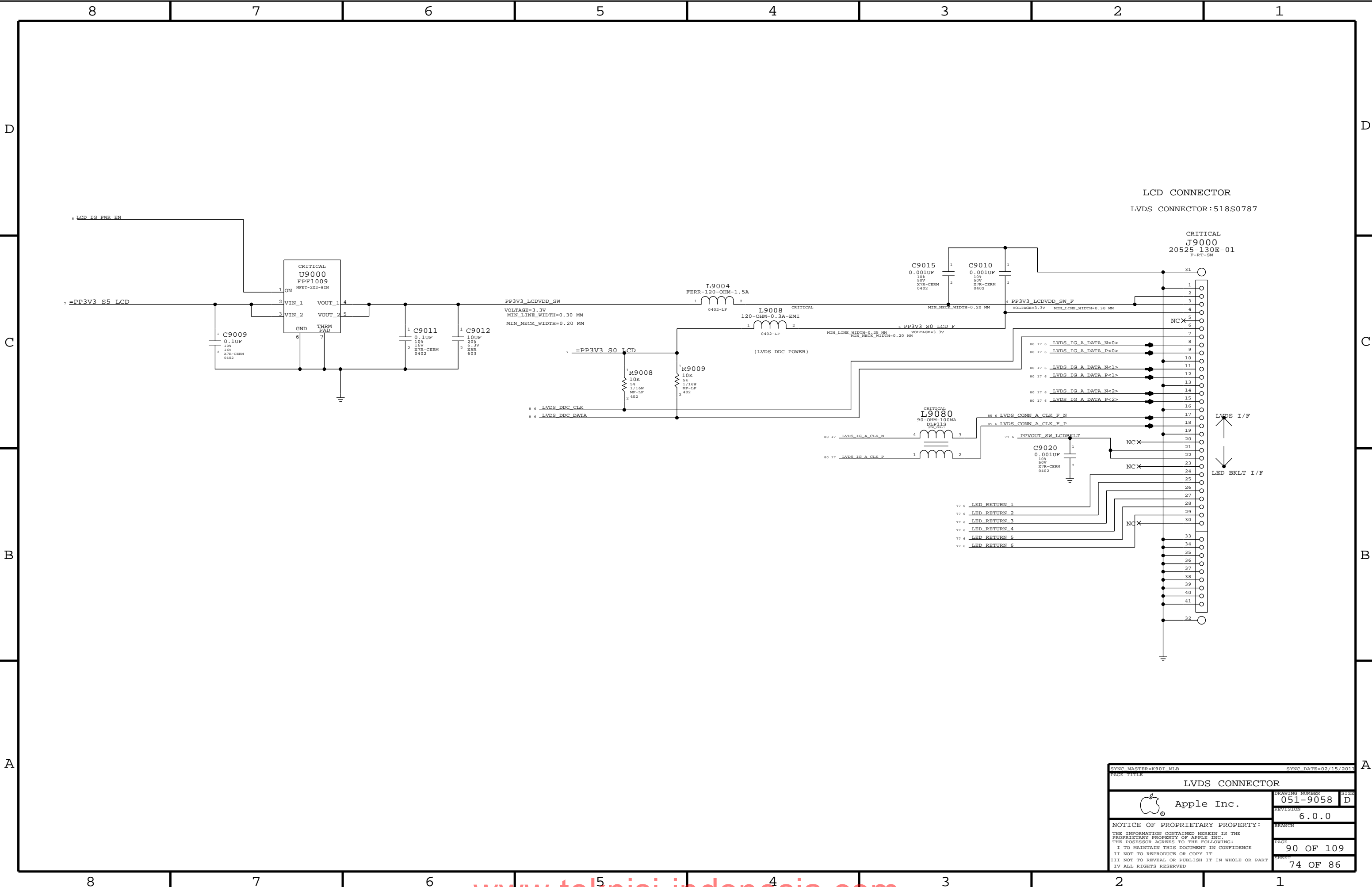
Vout = 1.05V
Max Current = 0.35A




SYNC MASTER=JACK J30		SYNC DATE=07/28/2011	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	051-9058
		REVISION	6.0.0
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SYNC MASTER=K901 MLB		SYNC DATE=02/15/2011	
PAGE TITLE			
LVDS CONNECTOR			
 Apple Inc.	DRAWING NUMBER		SIZE
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8	7	6	5	4	3	2	1
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D

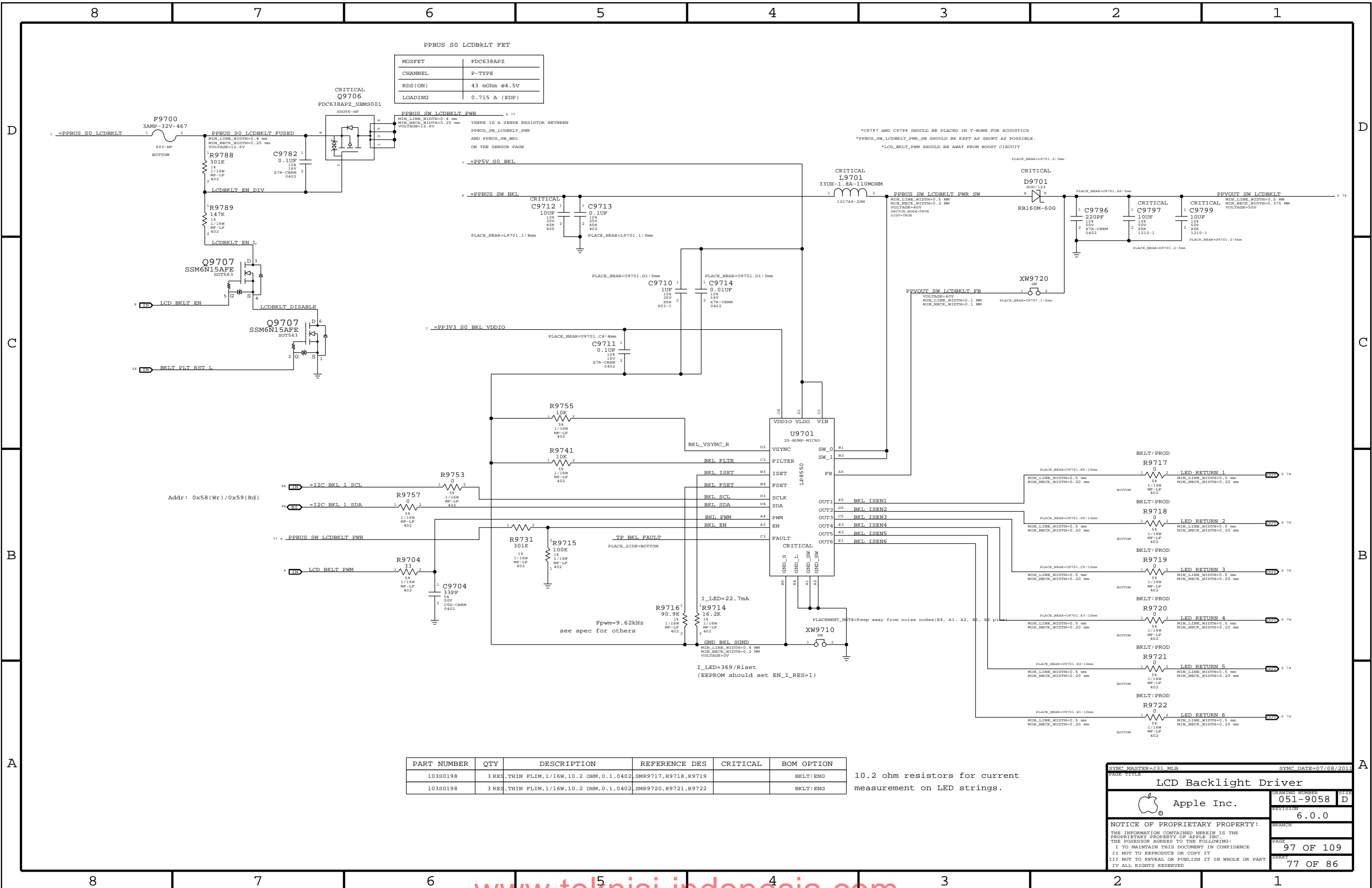
B

D

C


B

A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3 RES	THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402	SMR9717, R9718, R9719		BKLT:ENG
103S0198	3 RES	THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402	SMR9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=J31 MLB		SYNC DATE=07/08/2011	
PAGE TITLE			
LCD Backlight Driver			
 Apple Inc.		DRAWING NUMBER	051-9058
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D

CB

A

B

A

A

D

CB

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?	T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

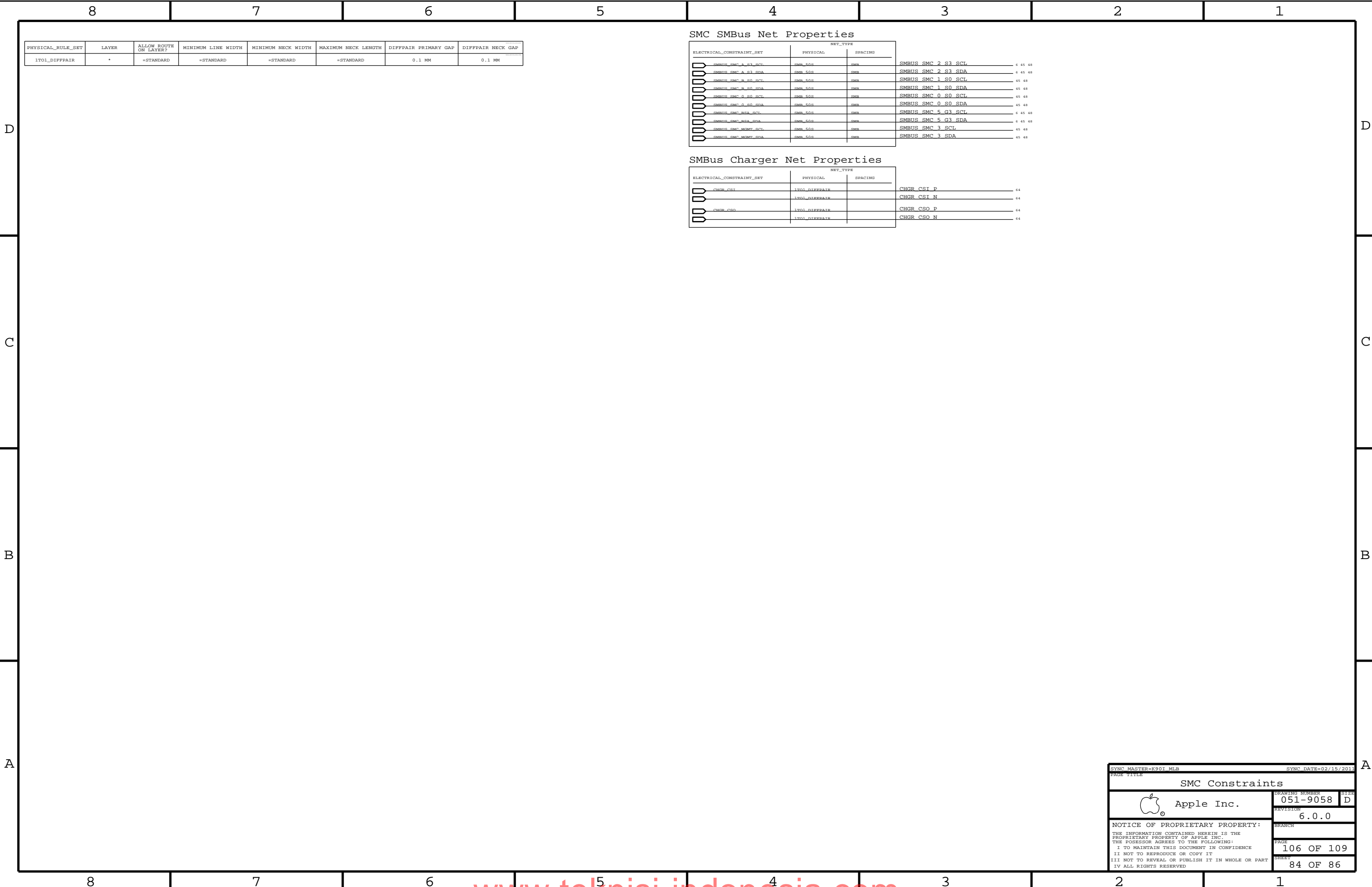
ELECTRICAL_CONSTRAINT_SET	NET TYPE			
	PHYSICAL	SPACING		
DP29	DP_85D	DP_ECH_TX	DP T29SNK0 ML C P<3..0>	33
DP29	DP_85D	DP_ECH_TX	DP T29SNK0 ML C N<3..0>	33
DP29	DP_T29SNK0_ML	DP_ECH_TX	DP T29SNK0 ML P<3..0>	33
DP29	DP_T29SNK0_ML	DP_ECH_TX	DP T29SNK0 ML N<3..0>	33
DP29	DP_85D	DP_ECH	DP T29SNK0 AUXCH C P	33
DP29	DP_85D	DP_ECH	DP T29SNK0 AUXCH C N	33
DP29	DP_T29SNK0_AUXCH	DP_ECH	DP T29SNK0 AUXCH P	33
DP29	DP_T29SNK0_AUXCH	DP_ECH	DP T29SNK0 AUXCH N	33
DP29	DP_85D	DP_ECH_TX	DP T29SNK1 ML C P<3..0>	33
DP29	DP_85D	DP_ECH_TX	DP T29SNK1 ML C N<3..0>	33
DP29	DP_T29SNK1_ML	DP_ECH_TX	DP T29SNK1 ML P<3..0>	33
DP29	DP_T29SNK1_ML	DP_ECH_TX	DP T29SNK1 ML N<3..0>	33
DP29	DP_85D	DP_ECH	DP T29SNK1 AUXCH C P	33
DP29	DP_85D	DP_ECH	DP T29SNK1 AUXCH C N	33
DP29	DP_T29SNK1_AUXCH	DP_ECH	DP T29SNK1 AUXCH P	33
DP29	DP_T29SNK1_AUXCH	DP_ECH	DP T29SNK1 AUXCH N	33
DP29	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>	33
DP29	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>	33
DP29	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P	33
DP29	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N	33
DP29	T29_I2C_55S	T29_I2C	I2C T29_SCL	33 48
DP29	T29_I2C_55S	T29_I2C	I2C T29_SDA	33 48
DP29	T29_SPT_CLK	T29_SPT	T29 SPI_CLK	33
DP29	T29_SPT_MOSI	T29_SPT	T29 SPI_MOSI	33
DP29	T29_SPT_MISO	T29_SPT	T29 SPI_MISO	33
DP29	T29_SPT_CS_L	T29_SPT	T29 SPI_CS_L	33
DP29	T29DP_80D	T29DP	T29 R2D C P<3..0>	33 76
DP29	T29DP_80D	T29DP	T29 R2D C N<3..0>	33 76
DP29	T29DP_100D	T29DP	T29 D2R P<3..0>	33 76
DP29	T29DP_100D	T29DP	T29 D2R N<3..0>	33 76

Only used on hosts supporting T29 video-in

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
R1	T29_R2D0	T29DP 80D	T29DP	T29 R2D P<0>
R2	T29_R2D0	T29DP 80D	T29DP	T29 R2D N<0>
R3	T29_R2D1	T29DP 80D	T29DP	T29 R2D P<1>
R4	T29_R2D1	T29DP 80D	T29DP	T29 R2D N<1>
R5		T29DP 80D	T29DP	T29 R2D C F P<1...0>
R6		T29DP 80D	T29DP	T29 R2D C F N<1...0>
R7	T29_D2R0	T29DP 100D	T29DP	T29 D2R C P<0>
R8	T29_D2R0	T29DP 100D	T29DP	T29 D2R C N<0>
R9	T29_D2R1	T29DP 100D	T29DP	T29 D2R C P<1>
R10	T29_D2R1	T29DP 100D	T29DP	T29 D2R C N<1>
R11		T29DP 100D	T29DP	T29DPA D2R1 AUXCH P
R12		T29DP 100D	T29DP	T29DPA D2R1 AUXCH N
R13		T29DP 80D	T29DP	DP SDRVA ML C P<3...0>
R14		T29DP 80D	T29DP	DP SDRVA ML C N<3...0>
R15		T29DP 80D	T29DP	DP SDRVA ML R P<3...0>
R16		T29DP 80D	T29DP	DP SDRVA ML R N<3...0>
R17	DP_SDRVA_ML_EVEN	T29DP 80D	T29DP	DP SDRVA ML P<2...0:2>
R18	DP_SDRVA_ML_EVEN	T29DP 80D	T29DP	DP SDRVA ML N<2...0:2>
R19	DP_SDRVA_ML_ODD	T29DP 80D	T29DP	DP SDRVA ML P<3...1:2>
R20	DP_SDRVA_ML_ODD	T29DP 80D	T29DP	DP SDRVA ML N<3...1:2>
R21	DP_SDRVA_AUXCH	T29DP 80D	T29DP	DP SDRVA AUXCH P
R22	DP_SDRVA_AUXCH	T29DP 80D	T29DP	DP SDRVA AUXCH N
R23		T29DP 80D	T29DP	DP SDRVA AUXCH C P
R24		T29DP 80D	T29DP	DP SDRVA AUXCH C N
R25		T29DP 80D	T29DP	T29DPA ML P<3...0>
R26		T29DP 80D	T29DP	T29DPA ML N<3...0>
R27		T29DP 80D	T29DP	T29DPA ML C P<3...0>
R28		T29DP 80D	T29DP	T29DPA ML C N<3...0>
R29		T29DP 80D	T29DP	DP A EXT AUXCH P
R30		T29DP 80D	T29DP	DP A EXT AUXCH N
R31	T29_R2D2	T29DP 80D	T29DP	T29 R2D P<2>
R32	T29_R2D2	T29DP 80D	T29DP	T29 R2D N<2>
R33	T29_R2D3	T29DP 80D	T29DP	T29 R2D P<3>
R34	T29_R2D3	T29DP 80D	T29DP	T29 R2D N<3>
R35		T29DP 80D	T29DP	T29 R2D C F P<3...2>
R36		T29DP 80D	T29DP	T29 R2D C F N<3...2>
R37	T29_D2R2	T29DP 100D	T29DP	T29 D2R C P<2>
R38	T29_D2R2	T29DP 100D	T29DP	T29 D2R C N<2>
R39	T29_D2R3	T29DP 100D	T29DP	T29 D2R C P<3>
R40	T29_D2R3	T29DP 100D	T29DP	T29 D2R C N<3>
R41		T29DP 100D	T29DP	T29DPB D2R3 AUXCH P
R42		T29DP 100D	T29DP	T29DPB D2R3 AUXCH N
R43		T29DP 80D	T29DP	DP SDRVB ML C P<3...0>
R44		T29DP 80D	T29DP	DP SDRVB ML C N<3...0>
R45		T29DP 80D	T29DP	DP SDRVB ML R P<3...0>
R46		T29DP 80D	T29DP	DP SDRVB ML R N<3...0>
R47	DP_SDRVB_ML_EVEN	T29DP 80D	T29DP	DP SDRVB ML P<2...0:2>
R48	DP_SDRVB_ML_EVEN	T29DP 80D	T29DP	DP SDRVB ML N<2...0:2>
R49	DP_SDRVB_ML_ODD	T29DP 80D	T29DP	DP SDRVB ML P<3...1:2>
R50	DP_SDRVB_ML_ODD	T29DP 80D	T29DP	DP SDRVB ML N<3...1:2>
R51	DP_SDRVB_AUXCH	T29DP 80D	T29DP	DP SDRVB AUXCH P
R52	DP_SDRVB_AUXCH	T29DP 80D	T29DP	DP SDRVB AUXCH N
R53		T29DP 80D	T29DP	DP SDRVB AUXCH C P
R54		T29DP 80D	T29DP	DP SDRVB AUXCH C N
R55		T29DP 80D	T29DP	T29DPB ML P<3...0>
R56		T29DP 80D	T29DP	T29DPB ML N<3...0>
R57		T29DP 80D	T29DP	T29DPB ML C P<3...0>
R58		T29DP 80D	T29DP	T29DPB ML C N<3...0>
R59		T29DP 80D	T29DP	DP B EXT AUXCH P
R60		T29DP 80D	T29DP	DP B EXT AUXCH N

Only used on dual-port hosts.



PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1To1_DiffPair	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_G3_SCL	SMB_50G	SMB	SMBUS_SMC_2_G3_SCL	6 45 48
SMBUS_SMC_A_G3_SDA	SMB_50G	SMB	SMBUS_SMC_2_G3_SDA	6 45 48
SMBUS_SMC_B_G0_SCL	SMB_50G	SMB	SMBUS_SMC_1_G0_SCL	45 48
SMBUS_SMC_B_G0_SDA	SMB_50G	SMB	SMBUS_SMC_1_G0_SDA	45 48
SMBUS_SMC_D_G0_SCL	SMB_50G	SMB	SMBUS_SMC_0_G0_SCL	45 48
SMBUS_SMC_D_G0_SDA	SMB_50G	SMB	SMBUS_SMC_0_G0_SDA	45 48
SMBUS_SMC'_5_G3_SCL	SMB_50G	SMB	SMBUS_SMC'_5_G3_SCL	6 45 48
SMBUS_SMC'_5_G3_SDA	SMB_50G	SMB	SMBUS_SMC'_5_G3_SDA	6 45 48
SMBUS_SMC'_MGMT_SCL	SMB_50G	SMB	SMBUS_SMC'_3_SCL	45 48
SMBUS_SMC'_MGMT_SDA	SMB_50G	SMB	SMBUS_SMC'_3_SDA	45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1To1_DiffPair		CHGR_CSI_P	64
CHGR_CSI	1To1_DiffPair		CHGR_CSI_N	64
CHGR_CSO	1To1_DiffPair		CHGR_CSO_P	64
CHGR_CSO	1To1_DiffPair		CHGR_CSO_N	64

SYNC_MASTER=K901_MLB

SYNC_DATE=02/15/2013

SMC Constraints

Apple Inc.

DRAWING_NUMBER051-9058

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1701_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_1701_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONS	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	-STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	QND	*	QND_P2984
MEM_CND	QND	*	QND_P2984
MEM_CTLG	QND	*	QND_P2984
MEM_DATA	QND	*	QND_P2984
MEM_PQS	QND	*	QND_P2984

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2004

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCTIE	*	GND_P2046
GND	PCTIE*	*	GND_P2049
GND	SATA*	*	GND_P2046
GND	USB*	*	GND_P2049
SR_POWER	CLK_PCTIE	*	PWR_P2046
SR_POWER	SATA*	*	PWR_P2049
SR_POWER	SATA*	*	PWR_P2046

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	LVSIS*	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

J30 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		MST_TYPE		SPACING		
		PHYSICAL				
		ENET_10G	ENETCONN	ENETCONN P<3..0>		37
		ENET_10G	ENETCONN	ENETCONN N<3..0>		37
		SATA_90D	SATA_RCH_RV	SATA_00D_D2R_C_P		6
		SATA_90D	SATA_RCH_RV	SATA_00D_D2R_C_N		6 41
		SATA_90D	SATA3_RCH_RV	SATA_HDD_D2R_RROUT_P		41
		SATA_90D	SATA3_RCH_RV	SATA_HDD_D2R_RROUT_N		41
		SATA_90D	SATA3_RCH_TV	SATA_HDD_R2D_RRIN_P		41
		SATA_90D	SATA3_RCH_TV	SATA_HDD_R2D_RRIN_N		41
899		SATA_90D	SATA3_RCH_TV	SATA_HDD_D2R_RRIN_P		41
900		SATA_90D	SATA3_RCH_TV	SATA_HDD_D2R_RRIN_N		41
901		SATA_90D	SATA3_RCH_TV	SATA_HDD_R2D_RROUT_P		41
902		SATA_90D	SATA3_RCH_TV	SATA_HDD_R2D_RROUT_N		41
		THRM_1001_500	THRMN	THMNSN D1_P		51
		THRM_1001_500	THRMN	THMNSN D1_N		51
		THRM_1001_500	THRMN	THMNSN D2_P		51
		THRM_1001_500	THRMN	THMNSN D2_N		51
		THRM_1001_500	THRMN	T29_THRMD_P		51
		THRM_1001_500	THRMN	T29_THRMD_N		51
		THRM_1001_500	THRMN	T29THMNSN D2_P		
		THRM_1001_500	THRMN	T29THMNSN D2_N		
		ISNS_1001_500	ISNSP	ISNS_HS_COMPUTING_N		50
		ISNS_1001_500	ISNSP	ISNS_HS_COMPUTING_P		50
		ISNS_1001_500	ISNSP	ISNS_HS_OTHER_N		50
		ISNS_1001_500	ISNSP	ISNS_HS_OTHER_P		50
		ISNS_1001_500	ISNSP	CPUVCCIOS0_CS_N		49 70
		ISNS_1001_500	ISNSP	CPUVCCIOS0_CS_P		49 70
		ISNS_1001_500	ISNSP	CPUIMVP ISNS1_P		49 68
		ISNS_1001_500	ISNSP	CPUIMVP ISNS1_N		49 68
		ISNS_1001_500	ISNSP	CPUIMVP ISNS2_P		49 68
		ISNS_1001_500	ISNSP	CPUIMVP ISNS2_N		49 68
		ISNS_1001_500	ISNSP	CPUIMVP ISNS1G_P		49 68
		ISNS_1001_500	ISNSP	CPUIMVP ISNS1G_N		49 68
903		ISNS_1001_500	ISNSP	CPUIMVP ISNS2G_P		49 68
904		ISNS_1001_500	ISNSP	CPUIMVP ISNS2G_N		49 68
		ISNS_1001_500	ISNSP	CPUIMVP ISUM_R_P		49
		ISNS_1001_500	ISNSP	CPUIMVP ISUM_R_N		49
		ISNS_1001_500	ISNSP	CPUIMVP ISUMG_R_P		49
		ISNS_1001_500	ISNSP	CPUIMVP ISUMG_R_N		49
905		ISNS_1001_500	ISNSP	CPUIMVP ISNSG_P		49
906		ISNS_1001_500	ISNSP	CPUIMVP ISNSG_N		49
		ISNS_1001_500	ISNSP	CPUIMVP ISNS_P		49
		ISNS_1001_500	ISNSP	CPUIMVP ISNS_N		49
907		ISNS_1001_500	ISNSP	VCCBARG_CS_P		65
908		ISNS_1001_500	ISNSP	VCCBARG_CS_N		65
		ISNS_1001_500	ISNSP	CPUIMVP ISUMG_P		
909		ISNS_1001_500	ISNSP	CPUIMVP ISUMG_N		68 69
910		ISNS_1001_500	ISNSP	CPU_THERMD_P		8 9
911		ISNS_1001_500	ISNSP	CPU_THERMD_N		8 9
912		ISNS_1001_500	ISNSP	ISNS_5V_50_HDD_N		49
913		ISNS_1001_500	ISNSP	ISNS_5V_50_HDD_P		49
914		ISNS_1001_500	ISNSP	ISNS_5V_50_HDD_R_N		49
915		ISNS_1001_500	ISNSP	ISNS_5V_50_HDD_R_P		49
916		ISNS_1001_500	ISNSP	ISNS_LCDBKLT_N		
917		ISNS_1001_500	ISNSP	ISNS_LCDBKLT_P		
		ISNS_1001_500	ISNSP	ISNS_LV5_53_DDR_P		49
918		ISNS_1001_500	ISNSP	ISNS_LV5_53_DDR_N		49
919		ISNS_1001_500	ISNSP	ISNS_LV5_53_DDR_R_P		49
920		ISNS_1001_500	ISNSP	ISNS_LV5_53_DDR_R_N		49
		LVDS_80D	LVDS_RCH_TV	LVDS_CONN A CLK_P_N		6 74
921		LVDS_80D	LVDS_RCH_TV	LVDS_CONN A CLK_P_P		6 74


J30 Specific Net Properties


ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SET_TYPE	
PCIE CLK100M AP	CLK PCIE SDD	CLK PCIE	PCIE CLK100M AP CONN P 6 32
	CLK PCIE SDD	CLK PCIE	PCIE CLK100M AP CONN N 6 32
	1T01 DIFFPAIR		CHGR CSI R P 64
	1T01 DIFFPAIR		CHGR CSI R N 64
	1T01 DIFFPAIR		CHGR CSO R P 64
	1T01 DIFFPAIR		CHGR CSO R N 64
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP L P OUT 6
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP L N OUT 6
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP SUB P OUT 6
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP SUB N OUT 6
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP R P OUT 6
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP R N OUT 6
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SSM2315 SUB N 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SSM2315 SUB P 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SSM2315 L N 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SSM2315 L P 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SSM2315 R N 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SSM2315 R P 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	AUD LO2 N R 57
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	AUD LO2 P R 57
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	AUD LO1 N R 57
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	AUD LO1 P R 57
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	AUD LO2 N L 57
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	AUD LO2 P L 57
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SPKRAMP INL P 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SPKRAMP INL N 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SPKRAMP INR P 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SPKRAMP INR N 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SPKRAMP INSUB P 60
SSM2315 AUD DIFF	1T01 DIFFPAIR	AUDIO	SPKRAMP INSUB N 60
USB TPAD	USB		USB TPAD R P 53
USB TPAD	USB		USB TPAD R N 53
FP1V1_50	SB POWER		FP1V1_50 6 7
FP1V1_50	SB POWER		FP1V1_50 6 7
FP1V5_036SD	SB POWER		FP1V5_036SD 6 7
GND	GND		GND

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

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Project Specific Constraints			
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		REVISION	6.0.0
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K90i Board-Specific Spacing & Physical Constraints							
BOARD LAYERS			BOARD AREAS		BOARD UNITS (MIL or MM)	ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA		MM	16.2	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	~50_OHM_SR	~50_OHM_SR	10 MM	0 MM	0 MM
STANDARD	*	Y	~DEFAULT	~DEFAULT	10 MM	~DEFAULT	~DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SR	TOP, BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SR	*	Y	0.080 MM	0.080 MM	~STANDARD	~STANDARD	~STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SR	TOP, BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SR	ISL10	N	0.126 MM	0.126 MM	~STANDARD	~STANDARD	~STANDARD
40_OHM_SR	ISL3, ISL4, ISL9	Y	0.126 MM	0.126 MM	~STANDARD	~STANDARD	~STANDARD
40_OHM_SR	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SR	TOP, BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SR	ISL10	N	0.145 MM	0.1 MM	~STANDARD	~STANDARD	~STANDARD
37_OHM_SR	ISL3, ISL4, ISL9	Y	0.145 MM	0.1 MM	~STANDARD	~STANDARD	~STANDARD
37_OHM_SR	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SR	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SR	*	Y	0.235 MM	0.2 MM	~STANDARD	~STANDARD	~STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SR	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SR	*	Y	0.070 MM	0.070 MM	~STANDARD	~STANDARD	~STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM
NOTE: These are Intel recommended impedances for PEG, unused on K90i.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SR	TOP, BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SR	*	Y	0.090 MM	0.090 MM	~STANDARD	~STANDARD	~STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
www.qdzbwx.com							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	~STANDARD	~STANDARD	~STANDARD	0.1 MM	0.1 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	~45_OHM_DIFF	~85_OHM_DIFF	~85_OHM_DIFF	~85_OHM_DIFF	~85_OHM_DIFF	~85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	~90_OHM_DIFF	~90_OHM_DIFF	~90_OHM_DIFF	~90_OHM_DIFF	~90_OHM_DIFF	~90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF	~100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_DIFF	*	N	~STANDARD	~STANDARD	~STANDARD	~STANDARD	~STANDARD
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.							
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